EDITORS' CHOICE

Epitaxial CVD Growth of Ultra-Thin Si Passivation Layers on Strained Ge Fin Structures

R. Loo,[1,*,z] H. Arimura,[1] D. Cott,[1] L. Witters,[1] G. Pourtois,[1,2,*] A. Schulze,[1] B. Douhard,[1] W. Vanherle,[1] G. Eneman,[1] O. Richard,[1] P. Favia,[1] J. Mitard,[1] D. Mocuta,[1] R. Langer,[1] and N. Collaert[1]

[1]Imec, B - 3001 Leuven, Belgium
[2]Department of Chemistry, Plasmant Research Group, University of Antwerp, B - 2610 Wilrijk-Antwerp, Belgium

Epitaxially grown ultra-thin Si layers are often used to passivate Ge surfaces in the high-k gate module of (strained) Ge FinFET and Gate All Around devices. We use Si_4H_{10} as Si precursor as it enables epitaxial Si growth at temperatures down to 330°C. C-V characteristics of blanket capacitors made on Ge virtual substrates point to the presence of an optimal Si thickness. In case of compressively strained Ge fin structures, the Si growth results in non-uniform and high strain levels in the strained Ge fin. These strain levels have been calculated for different shapes of the Ge fin and in function of the grown Si thickness. The high strain is the driving force for potential (unwanted) Ge surface reflow during Si deposition. The Ge surface reflow is strongly affected by the strength of the H-passivation during Si-capping and can be avoided by carefully selected process conditions.
© The Author(s) 2018. Published by ECS. This is an open access article distributed under the terms of the Creative Commons Attribution Non-Commercial No Derivatives 4.0 License (CC BY-NC-ND, http://creativecommons.org/licenses/by-nc-nd/4.0/), which permits non-commercial reuse, distribution, and reproduction in any medium, provided the original work is not changed in any way and is properly cited. For permission for commercial reuse, please email: oa@electrochem.org. [DOI: 10.1149/2.0191802jss]

Manuscript submitted December 12, 2017; revised manuscript received January 11, 2018. Published January 20, 2018. This was Paper 1150 presented at the National Harbor, Maryland Meeting of the Society, October 1–5, 2017.

The continuous scaling of CMOS devices requires new process developments because of the strong reduction of the allowable thermal budget for device processing. This is especially the case for narrow fin Field-Effect Transistors (FinFET) and vertically stacked Metal-Oxide-Semiconductor Field-Effect Transistors (MOSFET). New epitaxial growth schemes using higher order precursors are being assessed to enable epitaxial growth at the required reduced growth temperatures.[1–4] An example is the epitaxial Si growth on narrow Ge fins or on Ge nanowires to passivate (strained) Ge surfaces in the high-k gate module.[5–9] Si-passivation is advantageous over GeO_x-based gate stack in terms of Bias Temperature Instability (BTI) reliability.[10–14] Ge surface segregation during the epitaxial Si growth needs to be avoided as it leads to an increase of the interfacial trap density and distribution in the final gate stack.[10,15,16] On the other hand, the Si passivation layer has to be sufficiently thin. In the case of pFETs this is needed to approach an Equivalent Oxide Thickness (EOT) close to 1 nm and below as implemented in the current 14 nm-node devices.[10,16] For Ge nFETs, the lower conduction band (E_C) level in the Si might lead to an unwanted electron transport in the Si surface layer.[10] If the Si passivation layer is grown on compressively strained Ge FinFET structures or on horizontal strained Ge nanowires (gate-all-around devices), there is also a risk for Ge surface reflow during the Si deposition.[6,7,9] This in turn leads to a (partial) relaxation of the strained Ge layer. The resulting requirement for extremely low process temperatures during epitaxial Si growth (≤450°C) sets the need to use higher order Si-precursors such as Si_3H_8 or Si_4H_{10}.[7,15,17] Despite the use of these higher order precursors it is challenging to avoid the surface reflow of compressively strained Ge, especially for narrow fins and narrow Ge nanowires.[6,7,9]

In this manuscript, we discuss epitaxial Si growth by means of Chemical Vapor Deposition (CVD) at temperatures down to 330°C and using either trisilane (Si_3H_8) or tetrasilane (Si_4H_{10}) as Si precursor. Replacing Si_3H_8 by Si_4H_{10} results in ~40% higher growth rates. The growth rate also depends on the choice of the carrier gas and is affected by the underlying virtual substrate. The Si growth characteristics are discussed in view of its use for Ge surface passivation in the high-k gate module.[10,16,18] We use relaxed Ge fins for nFinFET devices and compressively strained Ge epitaxially grown on $Si_{0.3}Ge_{0.7}$ virtual substrates for pFinFET devices.[5–7,18,19] C-V characteristics were studied on blanket capacitors which were made after growing a thin Si passivation layer on Ge virtual substrates.

As mentioned before, there is a potential risk for surface reflow if the Si passivation layer is grown on compressively strained Ge fin structures. Three-dimensional atomistic modeling has been used to calculate the strain levels and strain distribution in the strained Ge fin. These calculations have been executed for different shapes of the Ge fin and in function of the grown Si thickness. X-ray Diffraction measurements (XRD), Reciprocal Space Mapping (RSM) and Nano Beam Diffraction (NBD) measurements were used to experimentally assess the strain formation during Si growth on strained Ge fins. It will be shown that the extremely large lattice mismatch between the Si passivation layer and the strained Ge fin leads to high and non-uniform strain levels in the Ge fin. This is the driving force for eventual Ge surface reflow during the Si deposition. Nevertheless, it is possible to avoid the Ge surface reflow by a careful optimization of the Si growth conditions.

Experimental

The epitaxial layers were grown in either ASM Epsilon or ASM Intrepid epi reactors. These are standard horizontal cold wall, load-locked RP-CVD single wafer systems designed for production applications. The ASM Epsilon is a stand-alone reactor and the ASM Intrepid is a cluster containing up to four process modules, including the Previum integrated low-temperature surface cleaning module. Si_4H_{10} and Silcore (a commercial grade of Si_3H_8) were used as Si precursors.

Si passivated Ge capacitors were fabricated on blanket Ge virtual substrates.[10,16] The Ge virtual substrates were grown on 300 mm blanket Si wafers.[20] After a post-epi thermal treatment at 850°C and Chemical Mechanical Polishing, the Ge virtual substrates were ~600 nm thick, with a threading dislocation density of 6–7 × 10^7 cm^{-2}. After conventional pre-epi cleaning ending with a wet HF treatment, the thin Si layer was epitaxially grown on the Ge surface. This was followed by a close-coupled dry O_3 oxidation at 300°C followed by 2–4 nm ALD HfO_2 deposition. For some devices, 0.3–0.5 nm PVD La was deposited on SiO_2 or on 1 nm HfO_2. Parts of the wafers received a laser anneal (LA) at 800°C. 5 nm ALD TiN and W were deposited as metal gate. Finally, the wafers received a H_2 sintering anneal at 400°C.

*Electrochemical Society Member.
zE-mail: roger.loo@imec.be

Downloaded on 2019-02-22 to IP 146.175.11.111 address. Redistribution subject to ECS terms of use (see ecsdl.org/site/terms_use) unless CC License in place (see abstract).

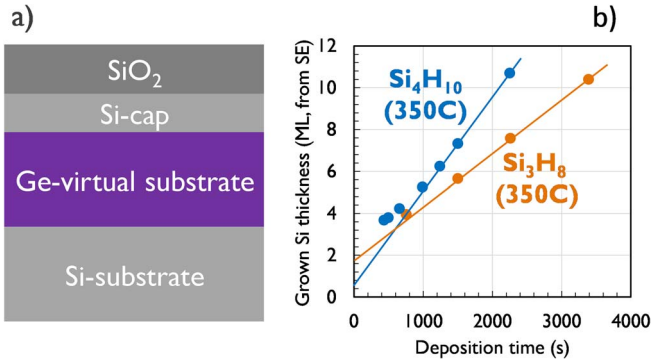

Figure 1. a) sample structure after deposition of a Si passivation layer on a blanket Ge virtual substrate followed by a close-coupled and controlled wet chemical oxidation of the Si surface. b) Si thickness as function of deposition time as extracted from SE for layers grown on 600 nm thick virtual Ge (001) substrates.

Results and Discussion

Epitaxial growth of ultra-thin Si passivation layers on blanket Ge surfaces.—Thickness extraction by Spectroscopic Ellipsometry. Ultrathin Si layers with thicknesses as used in real devices (3–10 ML) were grown on 300 mm blanket, relaxed (001) and (110) Ge virtual substrates which in turn were fabricated on Si wafers. The Si growth is followed by a close-coupled and controlled wet chemical oxidation of the Si surface after which the layers were measured by Spectroscopic Ellipsometry (SE) (Fig. 1a). The grown Si thickness is extracted from the sum of the measured Si thickness and the amount of Si consumed during surface oxidation. Figure 1b shows the extracted total Si thickness as function of deposition time as obtained on (001) oriented Ge surfaces and using either Si_4H_{10} or Si_3H_8 as Si precursor. The Si layers were grown at a nominal growth temperature of 350°C. As expected, the Si growth rate is higher if the layers are grown using Si_4H_{10}. For sufficiently long deposition times (>1000 s) meaning sufficiently thick Si layers (>5 ML), the Si thickness increases linearly with increasing deposition time. For shorter deposition times, the extracted Si thickness is apparently overestimated. This might be due to Ge segregation into the Si layer. If the Si-cap layer is too thin, the oxidation front comes close to or can even cross the Si/Ge interface resulting in the formation of a mixed SiGe-oxide during the post-deposition oxidation and an overestimation of the extracted Si layer. Indeed, thicker oxides are measured if the Si thickness is less than 5 ML. The faster oxidation reflects mixed and non-stoichiometric oxides. The extracted Si thicknesses are identical for Si grown on blanket Ge surfaces with (001) and (110) orientation, within the measurement accuracy (Table I). We therefore expect conformal growth if Si is grown on (strained) Ge fin structures. For Si growth with conventional precursors (SiH_4 or $SiCl_2H_2$), the growth rate varies in function of the the surface bond density resulting in different growth rates for different surface orientations.[21] The decomposition process is different for higher order precursors.[15,22] This might explain why the growth rate is independent from surface orientation.

Table I. Si thicknesses as extracted from SE for layers grown on Ge virtual substrates with (001) or (110) surface orientation using identical process conditions.

Deposition time (s)	Si thickness on Ge (001) in monolayers	Si thickness on Ge (110) in monolayers
493	not measured	4.2
1250	7.91	7.85
1500	9.23	not measured
2250	13.67	13.66

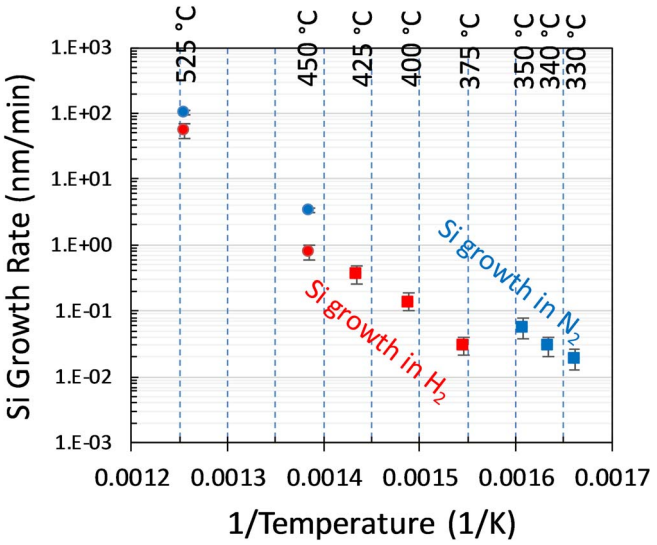

Figure 2. Si growth rate as function of nominal growth temperature using either N_2 (blue symbols) or H_2 (red symbols) as carrier gas and Si_4H_{10} as Si precursor. Layer thickness was measured by XRR (circles) for Si grown on strained $Si_{0.785}Ge_{0.215}$ and by SE (squares) for Si grown on Ge virtual substrates.

Temperature dependence of Si growth with Si_4H_{10}. Thicker Si layers were grown at higher deposition temperatures on strained $Si_{0.785}Ge_{0.215}$ and measured by X-Ray Reflectivity (XRR) to obtain the Arrhenius graphs shown in Figure 2. The data points obtained for temperatures ≤425°C have been obtained by SE on thin layers grown on top of relaxed Ge (blanket wafers). The Si growth rate is higher if N_2 is used as carrier gas, which has also been observed for other Si precursors.[23] The growth temperature can be reduced to 375°C (H_2) and 330°C (N_2), respectively. For the lowest temperatures, it is challenging to obtain a good within wafer uniformity (WIWU) in thickness but at 375°C or above standard deviations in thickness below 2% are easily obtained (49 data points over the wafer). The growth rates as measured for temperatures below 425°C are higher than expected from the temperate dependency at ≥ 450°C (Fig. 2) and the extracted activation energies seem to be lower as well (Table II). There might be some influence of the underlying virtual substrate on the Si growth rate. The epi tools used in this work are lamp heated systems and the real temperature on the growing surface can be different from the nominal temperature measured by thermocouples.[24] The composition and thickness of the virtual substrate can affect the temperature of the growing surface, which can be different depending on the characteristics of the starting layer. Indeed, slight variations in Si growth rate and WIWU were measured depending on the thickness of the Ge virtual substrate. The Si growth rate can also be affected by catalytic effects correlated with the composition of the underlying layer, especially during the initial stage of the growth.[25] In the initial stage of the Si growth, the growing surface changes from Ge (or SiGe) to SiGe with decreasing Ge content. The desorption rate of reaction by-products varies in function of the composition of the growing surface as the Si-H bound is stronger than the Ge-H bound.

Table II. Extracted Activation Energies for Si Growth.

Carrier gas	Temperature regime	Starting surface	Activation Energy
H_2	450–525°C	$Si_{0.785}Ge_{0.215}$	2.8 ± 0.2 eV
H_2	375–425°C	Ge	1.9 ± 0.4 eV
N_2	450–525°C	$Si_{0.785}Ge_{0.215}$	2.3 ± 0.1 eV
N_2	330–350°C	Ge	1.8 ± 0.4 eV

Downloaded on 2019-02-22 to IP 146.175.11.111 address. Redistribution subject to ECS terms of use (see ecsdl.org/site/terms_use) unless CC License in place (see abstract).

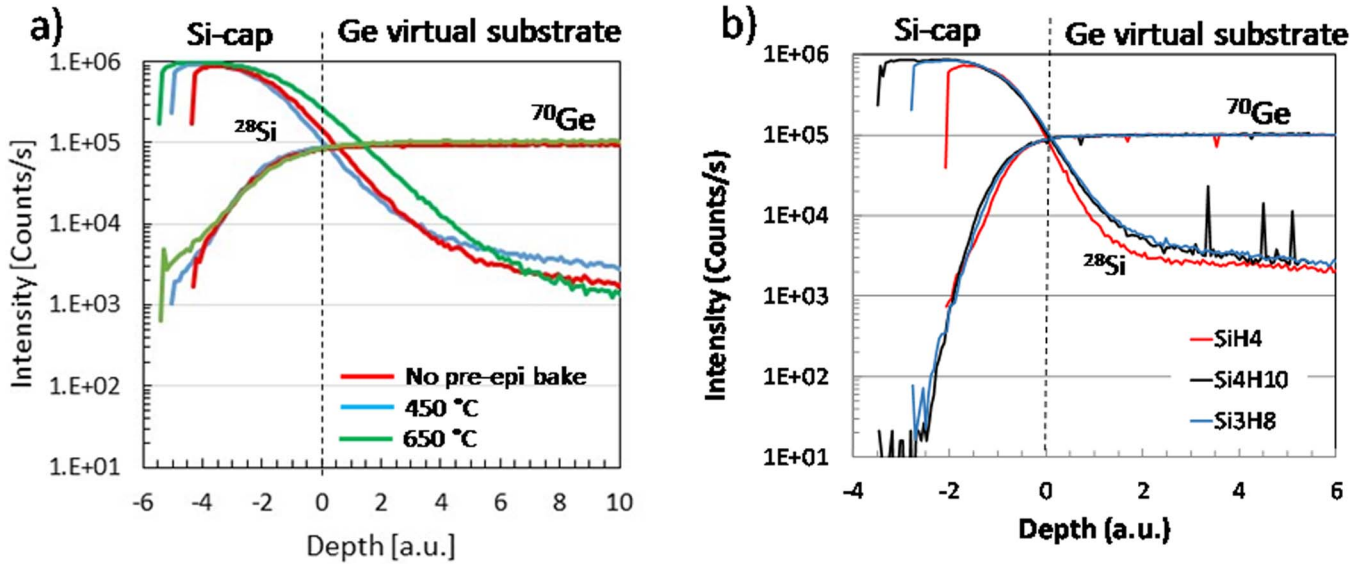

Figure 3. Comparison of Ge and Si depth profiles as measured by SIMS in ultra-thin Si layers epitaxially grown on relaxed Ge. Before Si growth, the wafer received a wet-chemical HF treatment. a) layers grown with SiH_4 comparing different pre-epi treatments and b) without pre-epi bake comparing different Si precursors. The growth temperature was 500°C in case of SiH_4 and 350°C in case of Si_3H_8 and Si_4H_{10}. (Fig. b has been previously published in Ref. 7).

Ge segregation into the Si-cap layer. Secondary-ion mass spectrometry (SIMS) measurements were used to study the Ge segregation from the Ge virtual substrate into the grown Si layer. In Figure 3, SIMS profiles were aligned at the Si-cap/Ge interface. Figure 3b shows the Si and Ge profiles for three samples, where the Si-cap layer was grown with three different Si precursors. The growth rate is different for the different process conditions, which explains the differences in Si thickness seen in Figure 3b. From previous work,[15,26] we learned that the Si and Ge gradients do not vary with deposition time (Si thickness). Therefore, we did not try to match the grown Si thicknesses for the different layers. In Fig. 3b, the slopes of the Ge profiles into the Si-cap layers are very similar which means that the Ge segregation into the Si cap layer is independent of the choice of the Si precursor.[7] The independence of the Ge segregation from the choice of the Si precursor is in contradiction with previous results, where we observed a higher Ge segregation if the Si is grown using SiH_4 or $SiCl_2H_2$.[15,26,27] The contradiction is caused by the use of different pre-epi treatments to remove the native oxide from the Ge starting surface. Previously, the native oxide on the Ge starting surface was removed by a pre-epi bake at $\geq$ 600°C. For the samples shown in Figure 3b, the oxide was removed by a wet-chemical treatment without in-situ bake. The effect of the pre-epi treatment on Ge surface segregation is seen in Figure 3a where we compare Ge segregation for Si layers grown with SiH_4 using different pre-epi bakes. For SiH_4, a less steep Ge profile reflecting enhanced Ge segregation from the Ge virtual substrate into the Si layer is indeed observed on samples that received a pre-epi bake at 650°C leaving a Ge surface without H-passivation. If the layers are grown with SiH_4 or $SiCl_2H_2$, the presence/absence of H-passivation on the starting and growing surface strongly affects the Ge segregation. This was previously predicted by Yang et al.[28] They used molecular-dynamics and first principle simulations to demonstrate that the Ge segregation to the growing surface occurring during the Si deposition is driven by the presence of chemisorbed hydrogen that governs the changes in surface energy between Si and Ge. In case of Si growth with SiH_4, the presence of H-passivation on the growing surface prevents the diffusion (segregation) of Ge toward the surface of the deposited Si films.[28] Without H-passivation, a more pronounced Ge segregation is predicted. If higher order Si precursors are used, the Si growth proceeds in a different growth mechanism[15] and the Ge surface segregation is not affected by the initial H passivation. According to Figure 3a, the grown Si thickness seems to vary on the pre-epi treatment. The origin has not been investigated. The differences in pre-epi treatment might lead to different surface passivation of the starting surfaces and also causing differences in the temperature of the reactor tube, which in turn might affect the growth rate at the given low growth temperature.[29]

Si-passivated Ge capacitors.—For Ge pFET devices, the passivation of the Ge surface using a thin Si layer is quite efficient. The valence band offset at the Si/Ge interface confines the holes in the Ge channel. High hole mobility strained Ge pFETs outperforming Si pFET devices have been demonstrated using Si passivated Ge surfaces.[5,6,18] For Ge nFETs, the concerns of using a thin Si passivation layer are the high D_{it} and the possible electron transport in the Si surface layer, as the conduction band (E_C) in Si is at a lower energetic level compared to Ge. Both concerns result in a reduced electron mobility.[10] G. Pourtois et al. showed that the effective E_C of the Si on Ge changes from a position lying deep inside the bandgap of the Ge for a thick remaining Si layer due to strain, toward the E_C of Ge for a thin remaining Si layer due to quantization.[10,30] Thus, to obtain the high electron mobility of Ge, the Si passivation layer needs to be sufficiently thin such that electrons are distributed in the Ge channel thanks to the limited physical thickness of the Si layer and to the quantization of the Si wavefunction. Si passivated Ge capacitors which were fabricated on blanket Ge virtual substrates showed very similar gate stack properties independent of the choice of the Si precursor gas, which was either Si_3H_8 or Si_4H_{10} (Fig. 4a). In Fig. 4a, we show D_{IT} of Si-passivated Ge gate stacks as function of CET thickness. The CET was extracted from the strong minority carrier response, where a contribution of the remaining Si thickness is included. The data point for Si_3H_8 is well in-line with the trend seen for Si_4H_{10}. Fig. 4b shows D_{IT} of Si-passivated Ge gate stacks as function of the initially grown Si thickness for Si grown with Si_3H_8. We like to mention that the gate stack was slightly different for both series of samples, but the oxidation process for forming the oxide interlayer was identical. The C-V characteristics and extracted D_{IT} values point to an optimal thickness of the Si passivation layer, for which D_{IT} is lowest (Fig. 4). If the Si layer is too thin, the O_3 oxidation reaches the Ge surface which results in degraded C-V characteristics. In addition, reduced carrier mobility and higher interface trap densities were reported for fully processed nFET devices.[10,16] On the other hand, the Si thickness should be kept as thin as possible to avoid electron transport in the Si-cap layer in case of nFET devices and to maintain low EOT values for pFET devices. On blanket capacitors, the controllability of the epitaxial Si growth is reflected in

Downloaded on 2019-02-22 to IP 146.175.11.111 address. Redistribution subject to ECS terms of use (see ecsdl.org/site/terms_use) unless CC License in place (see abstract).

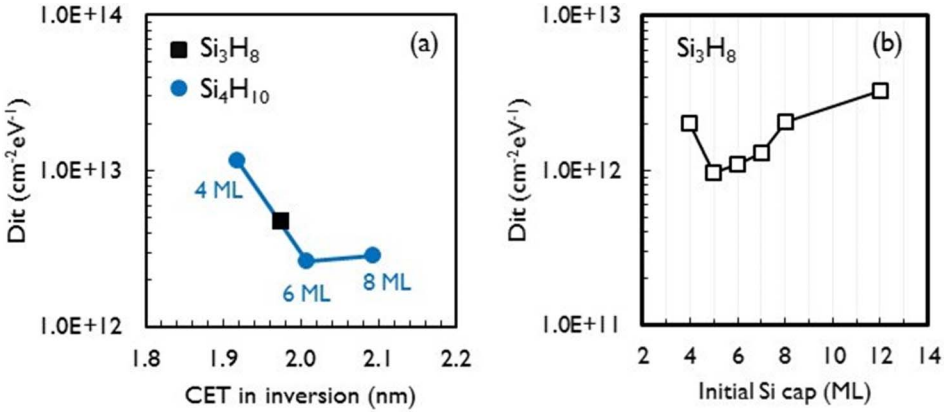

Figure 4. D_{IT} of Si-passivated Ge gate stacks a) as function of CET comparing Si layers grown with Si_3H_8 with Si_4H_{10} and b) as function of initially grown Si thickness for Si grown with Si_3H_8. Slightly different gate stacks were used for the samples in each figure, but the Si-cap and Si oxidation process was identical.

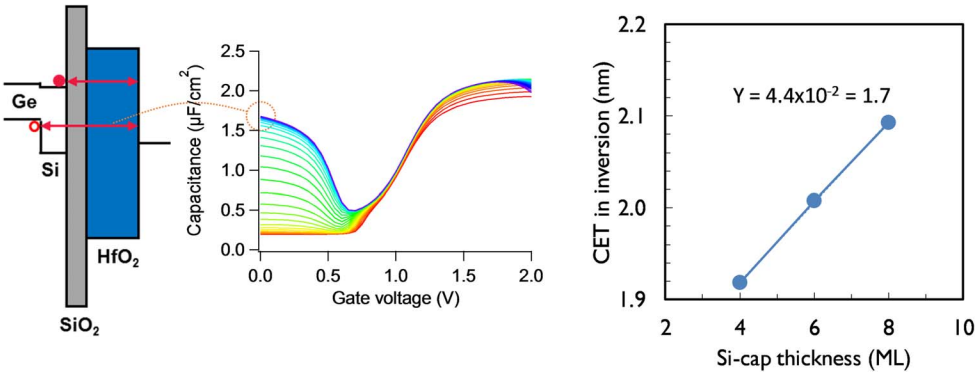

Figure 5. CET extracted in inversion mode from n-type Ge capacitors as function of the as-grown Si thickness. The Si passivation layer was growth with Si_4H_{10}.

the extracted values of the Capacitance Equivalent Thickness (CET) in inversion mode. For n-type capacitors, the CET value includes the remaining thickness of the Si passivation layer. The increase of the extracted CET thickness as function of the Si thickness as determined from SE measurements was estimated to 4.4×10^{-2} nm/ML (Fig. 5). When 11.9 is used as the k-value of Si, the estimated slope corresponds to an increase in Si physical thickness of 1.3×10^{-1} nm/ML which is very close to the theoretical value of the thickness of 1 ML Si (0.13125 nm).

Epitaxial growth of ultra-thin Si passivation layers on strained Ge fins.—Strained Ge FinFET structures fabricated on top of $Si_{0.3}Ge_{0.7}$ virtual substrates are normally uniaxially strained if the fin structures are sufficiently narrow (e.g. < 20 nm in width). They show compressive strain along the fin and (partial) elastic relaxation across the fin. Compressive uniaxial strain is preferred for pFET mobility and has been confirmed for the replacement channel fabrication scheme (STI first)[6,7,31] as well as the STI last fabrication scheme.[19,32] The out-of-plane lattice constant (in vertical direction) shows a larger lattice constant with respect to relaxed Ge, as verified by symmetric (004) ω -2Θ XRD scans.[32] After growing a 3–10 ML thick Si passivation layer on top of the strained Ge fin surfaces, the Ge peak shows a shift to smaller ω -2Θ (Fig. 6a). This reflects a reduction of the out-of-plane lattice parameter which in turn indicates a reduction of the in-plane strain value in the strained Ge fin structure. The shape of the strained Ge fin structure is clearly modified after the Si deposition as seen in the cross-sectional TEM images shown in Figure 6b, 6c. The reflow of the strained Ge fin and the strain loss are not observed if the wafer is exposed to the same thermal budget but without growing the Si layer. In addition, no surface reflow is observed if the Si layer is grown on strain relaxed Ge fins. Therefore, we believe that the observed relaxation and surface reflow of the strained Ge fin is caused during the deposition of the Si cap layer. The lattice mismatch of the Si grown on the fin side walls is more than 4.2% as the Ge is tensile strained in the vertical direction.

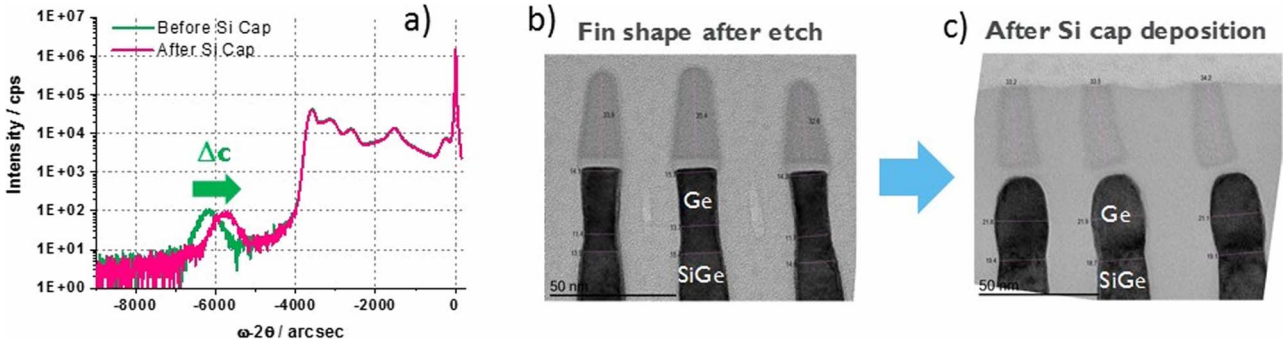

Figure 6. a) (004) ω -2Θ scans as measured before and after growing the Si passivation layer on top of strained Ge fins. b) and c) Cross-sectional TEM images showing the strained Ge fin shape before (b) and after (c) Si deposition.

Downloaded on 2019-02-22 to IP 146.175.11.111 address. Redistribution subject to ECS terms of use (see ecsdl.org/site/terms_use) unless CC License in place (see abstract).

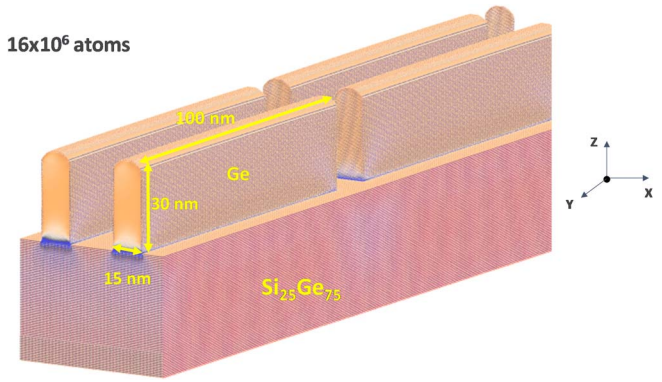

Figure 7. Scheme of the strained Ge fin structures for which the stress profiles have been calculated using three dimensional atomistic modeling.

The stress profiles in the Ge fins have been calculated using atomistic simulations based on the Tersoff pair potential.[33] The coordinates of the system were fully relaxed using a BFGS minimizer until a convergence with a maximum atomic force of 0.01 eV/Å is reached using the LAMMPS package.[34] The atomic stress profiles have been calculated within the virial approximation[35] and projected on the atomic volume of the relaxed Ge fins using a Voronoi tesselation scheme.[36] They were evaluated for free standing compressively strained Ge fins which are placed on a $Si_{0.25}Ge_{0.75}$ virtual substrate (Fig. 7). Rectangular and rounded fin structures with and without Si cap layer were considered. The fin width was set to 15 nm and the fin length to 100 nm. The model considers periodic boundaries. The methodology was benchmarked against TCAD synopsys sentaurus results to confirm its validity (Fig. 8). The calculated stress distribution within a strained Ge fin without Si capping shows a non-uniform distribution with enhanced strain relaxation across the Ge fins and compressive strain along the fins. At the fin edges, relaxation occurs also along the fins. The relaxation on the fin edges was experimentally confirmed by Nano Beam Diffraction (NBD) measurements. Figure 9 shows an

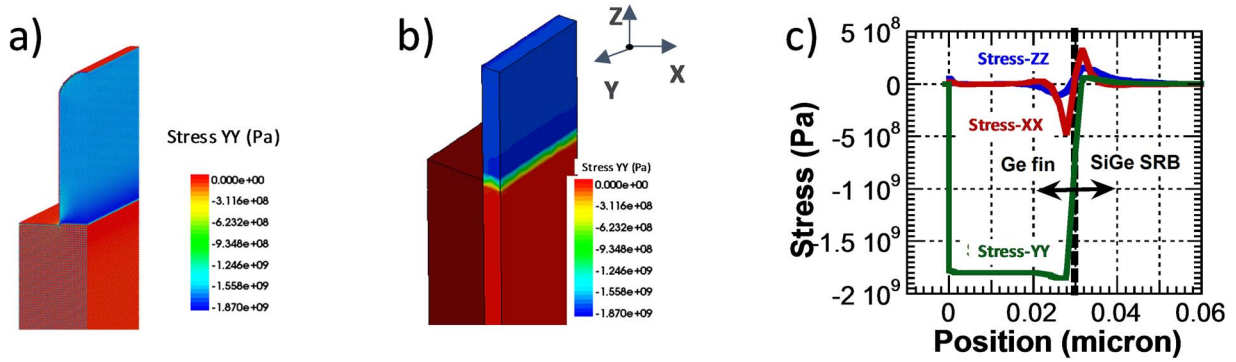

Figure 8. Stress profiles along the fin as calculated in the middle of the fin (far away from the fin edges) by a) 3-dimensional atomistic modeling and b) a 2-dimentional TCAD synopsys sentaurus simulation. c) Stress profiles in strained Ge fins as function of the distance from the $Si_{0.25}Ge_{0.75}$ virtual substrate and for diferent directions. Data have been obtained from the TCAD sentaurus synopsys simulator.

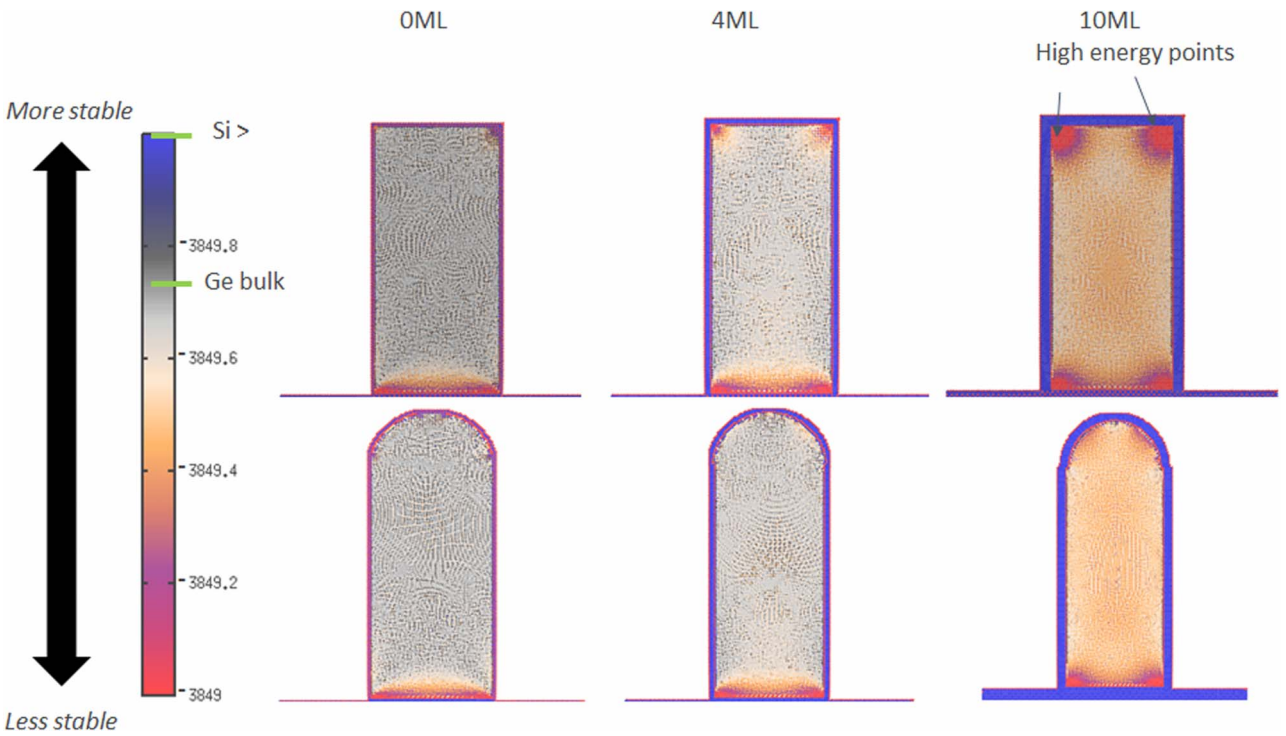

Figure 9. Atomic energy as calculated for strained Ge fins which are reactangular (top line) or rounded (bottom line) and capped with a Si passivation layer which is 0 ML, 4 ML, or 10 ML thick.

Downloaded on 2019-02-22 to IP 146.175.11.111 address. Redistribution subject to ECS terms of use (see ecsdl.org/site/terms_use) unless CC License in place (see abstract).

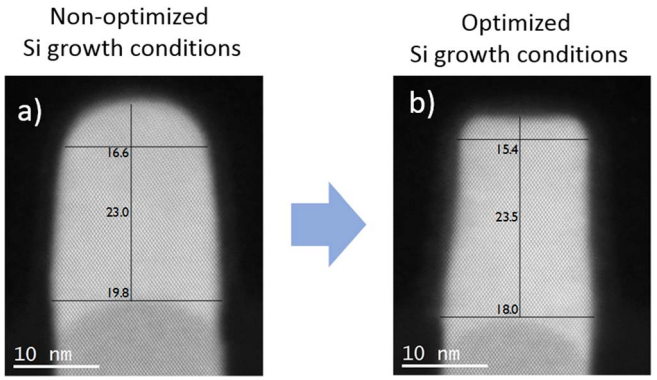

Figure 10. Cross-sectional TEM images showing strained Ge fins after deposition of the Si passivation layer. a) Non-optimized Si growth conditions. b) Optimized Si growth conditions allow to suppress strained Ge surface reflow.

illustration of the atomic energies as calculated for rectangular and rounded strained Ge fins without Si passivation layer and for strained Ge fins capped with 4 ML and 10 ML Si, respectively. Within the elastic regime, the non-uniformity as well as the absolute value of the calculated atomic energy (strain distribution in the Ge fin) increase with increasing Si thickness and the values are higher for the rectangular strained Ge fin structures. The rectangular fins show higher lateral and longitudinal stress gradients at the top corners and in the middle of the bottom of the fin. In addition, there is a shear stress along the YZ direction (not shown). The lower values of the atomic energy together with the lower stress gradient as calcultated for the rounded fin structures also indicate that the observed surface reflow of the strained Ge fin from a rectuanglar to a rounded fin is strain driven. Nevertheless, it is possible to suppress the surface reflow of the strained Ge fin structures during Si growth by carefully optimizing the epitaxial growth conditions, where it is important to maintain the H-passivation during the Si growth (Fig. 10). The effect of the H-passivation on the suppression of Ge surface reflow might be due to differences in surface energy. As mentioned earlier, Yang et al. concluded from molecular-dynamics simulations that surface Ge segregation occuring during the Si deposition is caused by changes in surface energy between Si and Ge.[28] In absence of H-passivation, Ge segregation during Si growth is expected to occur as Ge-Ge surface dimers are energetically the most stable.[28] If H-passivation is maintained, Si-Si dimers have the lowest energy and the H-passivation is expected to prevent Ge segregation toward the Si surface. SIMS measurements do not indicate the occurrence of Ge segregation during Si growth on strain relaxed blanket Ge surfaces (Fig. 3b). However, in the case of Si growth on compressively strained Ge fins, strain and strain relaxation play also an important role and Ge surface reflow is seen in Figures 6c and 10a where the same Si growth conditions were used as those of Figure 3b. A further improvement of the H-passivation during the Si growth enables to suppress the surface reflow of strained Ge fin structures (Fig. 10b) and horizontal strained Ge nanowires.[9]

Conclusions

We use Si_4H_{10} as Si precursor to enable epitaxial Si growth at temperatures down to 330°C. The Si growth characteristics are presented in view of Si passivation of Ge surfaces as used in the high-*k* gate module. Replacing Si_3H_8 by Si_4H_{10} results in ~40% higher growth rates. The growth rate also depends on the choice of the carrier gas and is affected by the underlying virtual substrate. Ge segregation into the Si layer has been studied for Si growth on blanket Ge surfaces. Ge segregation is suppressed if H-passivation is maintained during the Si deposition step. In that case, Ge segregation does not depend on the chosen Si precursor gas. C-V characteristics of blanket capacitors made on Ge virtual substrates point to the presence of an optimal Si thickness as on one hand one needs to avoid the formation of mixed SiGe-oxides and on the other hand, a too thick Si layer results in electron transport in the Si surface layer. The CET vs Si-cap slope nicely demonstrates the controllability of the epitaxial Si growth.

There is a potential risk for surface reflow if the Si passivation layer is grown on compressively strained Ge fin structures or on horizontal strained Ge nanowires as used in gate-all-around devices. Three-dimensional atomistic modeling has been used to calculate the strain levels and strain distribution in strained Ge fins. These calculations have been executed for different shapes of the Ge fin and in function of the grown Si thickness. High and non-uniform strain caused by the extremely large lattice mismatch between the Si passivation layer and the Ge fin is the driving force for potential Ge surface reflow during the Si deposition. The Ge surface reflow is strongly affected by the strength of the H-passivation during Si-capping and can be avoided by carefully selected process conditions.

Acknowledgments

The imec core CMOS program members, European Commission, the TAKEMI5 ECSEL project, local authorities and the imec pilot line are acknowledged for their support. This work was also part of a jdp with ASM. Air Liquide Advanced Materials is acknowledged for providing advanced precursor gases and Bruker Semiconductor Division for their kind support in XRD characterization of high mobility materials implemented in complex device architectures.

ORCID

R. Loo https://orcid.org/0000-0003-3513-6058

References

1. A. Hikavyy, I. Zyulkov, H. Mertens, L. Witters, R. Loo, and N. Horiguchi, *Mater. Sci. Semicond. Process.*, **70**, 24 (2017).
2. B. Vincent, R. Loo, W. Vandervorst, G. Brammertz, and M. Caymax, *J. Cryst. Growth*, **312**, 2671 (2010).
3. J. M. Hartmann, V. Benevemt, A. André, C. Sirisopanaporn, M. Veillerot, M. P. Samson, S. Barraud, Z. Essa, and B. Sermage, *ECS J. of Solid State Sci. Techn.*, **3**(11), 382 (2014).
4. M. Bauer and S. G. Thomas, *Thin Solid Films*, **520**, 3133 (2012).
5. L. Witters, J. Mitard, R. Loo, G. Eneman, H. Mertens, D. Brunco, S. Lee, N. Waldron, A. Hikavyy, P. Favia, A. Milenin, Y. Shimura, C. Vrancken, H. Bender, N. Horiguchi, K. Barla, A. Thean, and N. Collaert, *IEEE Int. Electron Dev. Meeting (IEDM), Tech. Dig.*, p. 534 (2013).
6. J. Mitard, L. Witters, Y. Sasaki, H. Arimura, A. Schulze, R. Loo, L. Ragnarsson, A. Hikavyy, D. Cott, T. Chiarella, S. Kubicek, H. Mertens, R. Ritzenthaler, C. Vrancken, P. Favia, H. Bender, N. Horiguchi, K. Barla, D. Mocuta, A. Mocuta, N. Collaert, and A. Thean, *2016 Symposium on VLSI Technology, Digest of Technical Papers*, p. 34.
7. R. Loo, A. Hikavyy, L. Witters, A. Schulze, H. Arimura, D. Cott, J. Mitard, C. Porret, H. Mertens, P. Ryan, J. Wall, K. Matney, M. Wormington, P. Favia, O. Richard, A. Thean, N. Horiguchi, and N. Collaert, *ECS J. of Solid State Sci. Techn.*, **6**(1), 14 (2017).
8. Y.-C. Yeo, X. Gong, M. J. H. van Dal, G. Vellianitis, and M. Passlack, *IEEE Int. Electron Dev. Meeting (IEDM), Tech. Dig.*, p. 28 (2015).
9. L. Witters, H. Arimura, F. Sebaai, A. Hikavyy, A. Milenin, R. Loo, A. De Keersgieter, G. Eneman, T. Schram, K. Wostyn, K. Devriendt, A. Schulze, R. Lieten, S. Bilodeau, E. Cooper, P. Storck, E. Chiu, C. Vrancken, P. Favia, E. Vancoille, J. Mitard, R. Langer, A. Opdebeeck, F. Holsteyns, N. Waldron, K. Barla, V. De Heyn, D. Mocuta, and N. Collaert, *IEEE Trans. On Electr. Devices*, **64**(11), 4587 (2017).
10. H. Arimura, S. Sioncke, D. Cott, J. Mitard, T. Conard, W. Vanherle, R. Loo, P. Favia, H. Bender, J. Meersschaut, L. Witters, H. Mertens, J. Franco, L. Ragnarsson, G. Pourtois, M. Heyns, A. Mocuta, N. Collaert, and A. Thean, *IEEE Int. Electron Dev. Meeting (IEDM), Tech. Dig.*, p. 588 (2015).
11. J. Franco, B. Kaczer, P. Roussel, J. Mitard, S. Sioncke, L. Witters, H. Mertens, T. Grasser, and G. Groeseneken, *IEEE Int. Electron Dev. Meeting (IEDM), Tech. Dig.*, p. 397 (2013).
12. C. Lu, C. H. Lee, T. Nishimura, and A. Toriumi, *2015 Symposium on VLSI Technology, Digest of Technical Papers*, p. 18.
13. S. Takagi, M. ke, C.-Y. Chang, C. Yokoyama, M. Yokoyma, T. Gotow, K. Nishi, S.-H. Yoon, and M. Takenaka, *ECS Trans*, **80**(1), 109 (2017).
14. M. Ke, M. Takenaka, and S. Takagi, *Proceedings of the 47th European Solid-State Device Research Conference (ESSDERC)*, p. 296 (2017).
15. M. Caymax, F. Leys, J. Mitard, K. Martens, L. Yang, G. Pourtois, W. Vandervorst, M. Meuris, and R. Loo, *J. Electrochem. Soc.*, **156**(12), H979 (2009).
16. H. Arimura, D. Cott, R. Loo, W. Vanherle, Q. Xie, F. Tang, X. Jiang, J. Franco, S. Sioncke, L. Ragnarsson, E. Chiu, X. Lu, J. Geypen, H. Bender, J. Maes, M. Givens,

Downloaded on 2019-02-22 to IP 146.175.11.111 address. Redistribution subject to ECS terms of use (see ecsdl.org/site/terms_use) unless CC License in place (see abstract).

A. Sibaja-Hernandez, K. Wostyn, G. Boccardi, J. Mitard, N. Collaert, and D. Mocuta, *IEEE Int. Electron Dev. Meeting (IEDM), Tech. Dig.*, p. 834 (2016).
17. B. Vincent, L. Witters, O. Richard, A. Hikavyy, H. Bender, R. Loo, M. Caymax, and A. Thean, *ECS Trans*, **50**(9), 39 (2012).
18. H. Arimura, D. Cott, R. Loo, W. Vanherle, Q. Xie, F. Tang, X. Jiang, J. Franco, S. Sioncke, L. Ragnarsson, E. Chiu, X. Lu, J. Geypen, H. Bender, J. Maes, M. Givens, A. Sibaja-Hernandez, K. Wostyn, G. Boccardi, J. Mitard, N. Collaert, and D. Mocuta, *2017 Symposium on VLSI Technology, Digest of Technical Papers*, p. 196.
19. J. Mitard, L. Witters, R. Loo, S. Lee, J. Sun, J. Franco, L. Ragnarsson, A. Brand, X. Lu, N. Yoshido, G. Eneman, D. Brunco, M. Vorderwestner, P. Storck, A. Milenin, A. Hikavyy, N. Waldron, P. Favia, D. Vanhaeren, A. Vanderheyden, O. Richard, H. Mertens, H. Arimura, S. Sioncke, C. Vrancken, H. Bender, P. Eyben, K. Barla, S. Lee, N. Horiguchi, N. Collaert, and A. Thean, *2014 Symposium on VLSI Technology, Digest of Technical Papers*, p. 138.
20. P. Fakhimi, C. Porret, S. A. Srinivasan, R. Loo, and P. Berger, *10th International Conference on Silicon Epitaxy and heterostructures (ICSI-10), book of abstracts*, p. 191 (2017).
21. J. M. Hartmann, M. Burdin, G. Rolland, and T. Billon, *J. Crystal Growth*, **294**, 288 (2006).
22. J. J. Watkins, M. D. Sefcik, and M. A. Ring, *Inorg. Chem.*, **11**, 3146 (1972).
23. P. Meunier-Beillard, M. Caymax, K. Van Nieuwenhuysen, G. Doumen, B. Brijs, M. Hopstaken, L. Geenen, and W. Vandervorst, *Appl. Surf. Science*, **224**(1–4), 31 (2004).
24. W. B. De Boer, *ECS Trans*, **16**(10), 13 (2008).
25. R. Loo, H. Sorada, A. Inoue, B. Lee, S. Hyun, S. Jakschik, G. Lujan, T. Hoffmann, and M. Caymax, *Semicond. Sci. and Technol.*, **22**(1), S110 (2007).
26. B. Vincent, W. Vandervorst, M. Caymax, and R. Loo, *Appl. Phys. Lett.*, **95**, 262112 (2009).
27. B. Vincent, R. Loo, W. Vandervorst, J. Delmotte, B. Douhard, V. Valev, M. Vanbel, T. Verbiest, J. Rip, B. Brijs, T. Conard, C. Claypool, S. Takeuchi, S. Zaima, J. Mitard, B. De Jaeger, J. Dekoster, and M. Caymax, *Solid State Electronics*, **60**, 116 (2011).
28. Y. Yang, G. Pourtois, M. Caymax, A. Ceulemans, and M. Heyns, *Phys. Rev. B*, **79**, 165312 (2009).
29. Hichem M'Saad, presentation at ASM private luncheon seminar: *Advancing Epitaxy, San Francisco, December 6*, 2017.
30. G. Pourtois, M. Houssa, B. De Jaeger, B. Kaczer, F. Leys, M. Meuris, M. Caymax, G. Groeseneken, and M. Heyns, *Appl. Phys. Lett.*, **91**, 023506 (2007).
31. A. Schulze, R. Loo, P. Ryan, M. Wormington, P. Favia, W. Vandervorst, and M. Caymax, *Nanotechnology*, **28**, 145703 (2017).
32. A. Schulze, R. Loo, L. Witters, H. Mertens, A. Gawlik, N. Horiguchi, N. Collaert, M. Wormington, P. Ryan, W. Vandervorst, and M. Caymax, *Physica Status Solidi C*, 2017, 1700156.
33. J. Tersoff, *Phys. Rev. B*, **38**, 9902 (1988).
34. S. J. Plimpton, *J. Comp. Phys.*, **117**, 1 (1995).
35. R. Clausius, *Phil. Mag.*, **40**, 122 (1870).
36. F. Aurenhammer and R. Klein, "Voronoi Diagrams." Ch. *5 in Handbook of Computational Geometry* ,(Ed. J.-R. Sack and J. Urrutia,). Amsterdam, Netherlands: North-Holland, pp. 201, 2000.

Downloaded on 2019-02-22 to IP **146.175.11.111** address. Redistribution subject to ECS terms of use (see **ecsdl.org/site/terms_use**) unless CC License in place (see abstract).