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Design and simulation of plasmonic interference-based majority gate

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Major obstacles in current CMOS technology, such as the interconnect bottleneck and thermal heat management, can be overcome by employing subwavelength-scaled light in plasmonic waveguides and devices. In this work, a plasmonic structure that implements the majority (MAJ) gate function is designed and thoroughly studied through simulations. The structure consists of three merging waveguides, serving as the MAJ gate inputs. The information of the logic signals is encoded in the phase of transmitted surface plasmon polaritons (SPP). SPPs are excited at all three inputs and the phase of the output SPP is determined by the MAJ of the input phases. The operating dimensions are identified and the functionality is verified for all input combinations. This is the first reported simulation of a plasmonic MAJ gate and thus contributes to the field of optical computing at the nanoscale. [http://dx.doi.org/10.1063/1.4989817]

Electronic integrated circuit downscaling, dictated by Moore,[1] has been the driving factor of the semiconductor industry. However, when Moore's law ends, the ever increasing demand for energy-efficient and high performance computing will not. New transistor types are being developed to extend this law as far as possible, but improvements in charge-based devices will eventually come to an end.[2] Photonic technologies already provide data communication with the speed of light and complement the slower but very small electronics. The major issues in current CMOS technology are the interconnect bottleneck[3] and thermal heat management[4] which both may be overcome by employing light in the bottom layers of the circuit. To enable this, optical waveguides and devices must be scaled beyond the diffraction limit of light. This is where plasmonics comes into play by providing subwavelength-scale confinement while maintaining speeds in the order of the speed of light.

In the field of plasmonics, surface plasmon polaritons (SPPs) are of particular interest for wave computing applications. SPPs are electromagnetic waves coupled to electron oscillations, supported by a metal-dielectric interface. The characterizing dispersion relation for SPPs yields the subwavelength-scale confinement. The electric field amplitude of the SPP wave decays exponentially perpendicular to the direction of propagation. This decay depends on the material in which the SPP wave resides and it is, for example, very strong in metals and weaker in dielectrics. This difference in field decay is a key property for the confinement and guiding of SPPs.

Central in the field of plasmonics is the trade-off between confinement and propagation length of the propagating SPP waves. For a specific waveguide design, a large propagation length implies relatively poor confinement. This trade-off is valid for all materials and at all wavelengths and is extensively covered in various publications.[5] The group velocity of the SPP wave also decreases for

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larger propagation vectors. At first glance, this implies the number of cascaded devices and bandwidth are lower for strong confinement. However, besides denser parallel packing, a smaller wavelength sallows devices and interconnects to have a shorter length resulting in a higher number of cascaded devices for a constant length and lower delay.

Due to the above-mentioned trade-off there is a large variety in plasmonic waveguides,[5–9] each suited best for a certain application. Waveguide geometries such as metal-insulator-metal (MIM) provide relatively good confinement at small propagation lengths due to the fast electric field decay in the metal. Unlike MIM geometries, IMI geometries yield long propagation lengths at relatively poor confinement. These two waveguide geometries are very primitive but are the backbone for many other waveguides.

The physical phenomenon that enables wave computing is interference which causes superimposed waves to form one resulting wave. Further in this work, phase encoding of binary data into the phase of wave packets will be employed in simulations. Encoding a logic '1' and '0' in phase implies assigning a phase shift to the SPP wave for each of these values. A logic '1' imposes a phase shift of 0 and a logic '0' imposes a phase shift of π.[10]

To employ plasmonic interference devices in computing applications, a specific synthesis methodology is required which can realise a functional logic network incorporating these interference devices. One such methodology is called *majority-inverter graph* (MIG),[11] and it can exploit the properties of wave computing since majority (MAJ) gates and inverters emerge naturally from straightforward structures used in wave computing. A MAJ gate can be constructed by intersecting three waveguides and an inverter is a waveguide segment with a length of $\left(n + \frac{1}{2}\right)\lambda$.[12,13]

Due to the increased interest in optical computing at the nanoscale, some findings on plasmonic logic devices have already been published in recent years. These include simulations of plasmonic logic gates[14] and also experimental proof of functional single gates.[15] However, until now the publications have only been concerned with the conventional logic functions (AND,[16] OR,[16] NOT,[14] NAND,[14] NOR,[15] XOR[17] and XNOR[18]) and this research proposes a functional design for a MAJ gate, which so far has been lacking. The functionality of the design will be verified by simulating the MAJ operation and measuring the output state separation between a logic '1' and '0' for all possible input combinations.

All the results in this work are obtained in *Lumerical*, a commercial simulator based on the finite-difference time-domain (FDTD) method[19] which solves Maxwell's equations on a discrete spatiotemporal grid. A typical simulation environment is depicted in Figure 2. The environment contains input sources, different materials constituting the simulated structure and field monitors. In the $\hat{x}$-direction, the simulated structure is extended through 12 layers of absorbing perfectly matched layers (PML) to truncate the computational region. The PML layers were placed at a distance of one wavelength (1550 nm) from the mode sources and output monitors. In the $\hat{y}$ and $\hat{z}$-direction, the computational space was also ended with PML at a distance of one wavelength (1550 nm) from the outer edges of the simulated structure. This distance between the simulated structure and the PML makes sure all the electromagnetic fields fit into the simulation space. The required mesh density was obtained by starting from a coarse mesh and refining this mesh until the critical simulation parameter, the output amplitude, converged. This resulted in a cell size of 25 nm x 25 nm x 7.5 nm ($\hat{x}$ x $\hat{y}$ x $\hat{z}$) with axis orientation as given in Figure 2. The mesh must be denser in the $\hat{z}$-direction since the E_z-field is the strongest and most critical field. To ensure convergence, the simulation was stopped when the electromagnetic fields at the simulation boundary reached 10^{-8} of their initial value at t_0. Additionally it was verified no reflections or oscillations were occurring when the simulation was stopped. The waveguide employed in this work is a long-range dielectric-loaded surface plasmon polariton (LR-DLSPP) waveguide from Gosciniak et al.[9] and the cross-section of this waveguide is shown in Figure 1a. This waveguide is a hybrid between a long-range waveguide providing large propagation lengths and a dielectric loaded waveguide yielding good confinement. The dimensions and used materials for the waveguide are given in Table I. These dimensions are optimized for SPP propagation at a wavelength of 1550 nm and the fundamental plasmonic mode which is used for all simulations is shown in Figure 1b.

SPPs were excited by placing mode sources inside each input waveguide, exciting the fundamental plasmonic mode from Figure 1b (see simulation setup in Figure 2). Eventually in a fabricated

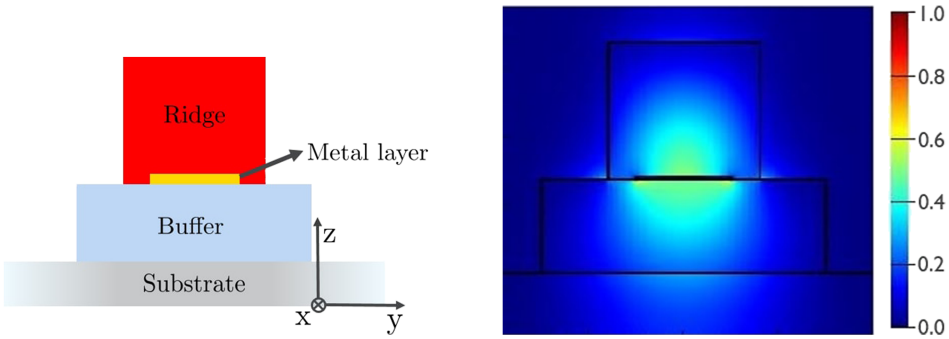


FIG. 1. (a) Cross section of the LR-DLSPP waveguide, reconstructed from Gosciniak et al.[9] and (b) Electric field intensity of corresponding fundamental mode.

TABLE I. Waveguide specifications.[9]

Waveguide section	Buffer	Metal layer	Ridge
Width (nm)	1500	500	800
Thickness (nm)	550	15	800
Material	SiO_2	Gold	BCB
Refractive index n	1.45	0.18+10.2i	1.535

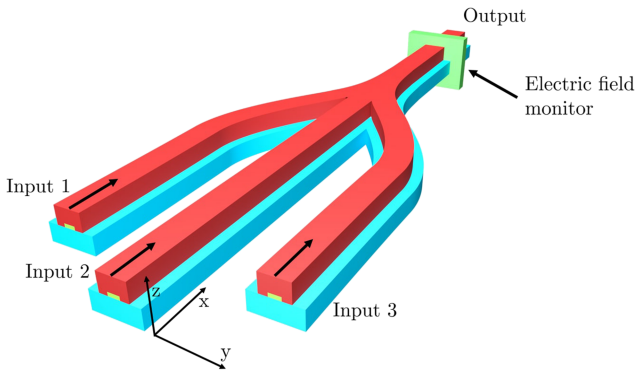


FIG. 2. Simulation setup with an example of a simulated structure, a source at each input and the electric field monitor at the output.

device, SPP waves can be excited by integrated plasmonic sources. One example is a vertical-cavity surface-emitting laser which couples to waveguided SPP modes.[20] The excited plasmonic mode can than serve as an input '1' by coupling it directly into an input waveguide or as an input '0' by propagating it half a wavelength longer or employing a phase-shifter. An even more compact approach would require electrical excitation which is currently being investigated.[21]

The excited input signal is a SPP wave packet with an equal amplitude for all inputs. A phase difference of zero was selected for a logic '1' and for a logic '0' the phase difference is π as depicted in Figure 3a. The SPP wave packet has a center frequency of 193 Thz as shown in Figure 3b.

The parameter to be detected is the phase of the output signal and this can be extracted from the time signal of the electric field monitor in the output waveguide as displayed in Figure 2. This signal is added to a reference signal (the input signal for a '1') representing an ideal '1'. The summation of these two signals gives the wave packet resulting from interference between the detected wave packet and the reference wave packet. This is done because at such high frequencies the phase of the wave packet can't be detected directly. In this work the interfered wave packet resulting from the output

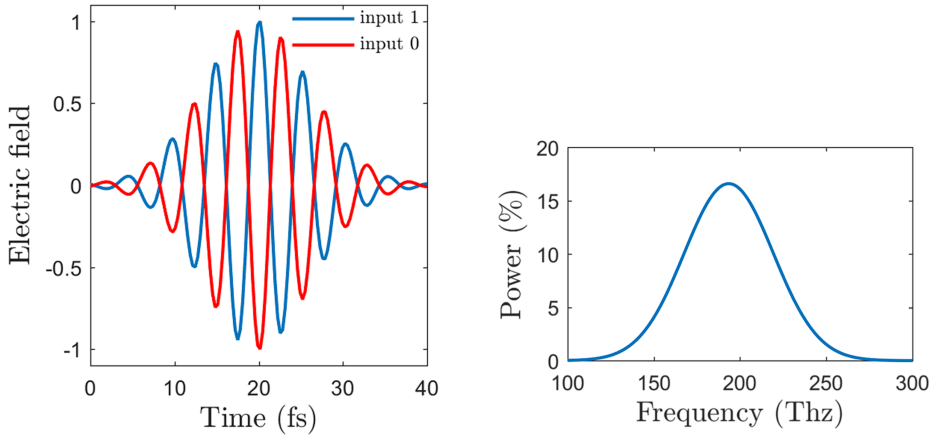


FIG. 3. Input signal characteristics, (a) Input time signals, (b) Frequency profile.

wave packet and reference wave packet was obtained by mathematically summing their related time signals.

It's essential the excited SPP wave packets travel the same distance before interfering to make sure they have the same phase relative to the phase at the input upon interference. In basic structures containing only straight waveguides this can be done by placing the sources at the same distance from the interference region. With designs employing bent waveguides this is not possible, but in this case the position of the sources can be adjusted by exciting each source separately and monitoring the phase of the output. Next the sources can be shifted in space or delayed in time until all the SPP waves have the same phase upon interference.

The measured output time signal and interfered signal can now be used to introduce a figure of merit (FOM) to characterize the measured output signal. This FOM rates the output signal based on the peak amplitudes of the electric field and is given in Equation (1). The used quantities here are the peak amplitudes of the reference signal and interfered signal.

$$\mathrm{FOM} = \frac{PA_i}{PA_r} \tag{1}$$

PA_i is the quantity to be eventually measured, and the FOM introduced above can be used to rate the performance of the MAJ gate. The difference between the lowest PA_i/PA_r for '1's and highest PA_i/PA_r for '0's is defined as the *output group state separation* Δ_{state} in Equation (2).

$$\begin{aligned}\Delta_{state} &= \min \mathrm{FOM}(111,110,101) \\ &- \max \mathrm{FOM}(000,001,010)\end{aligned} \tag{2}$$

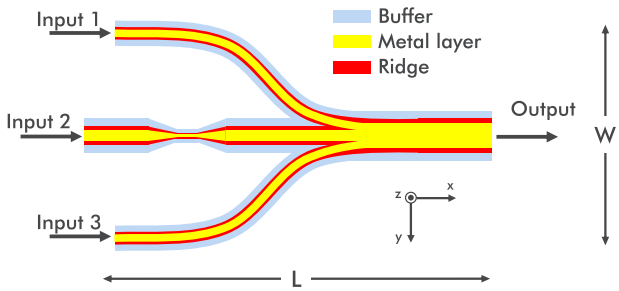
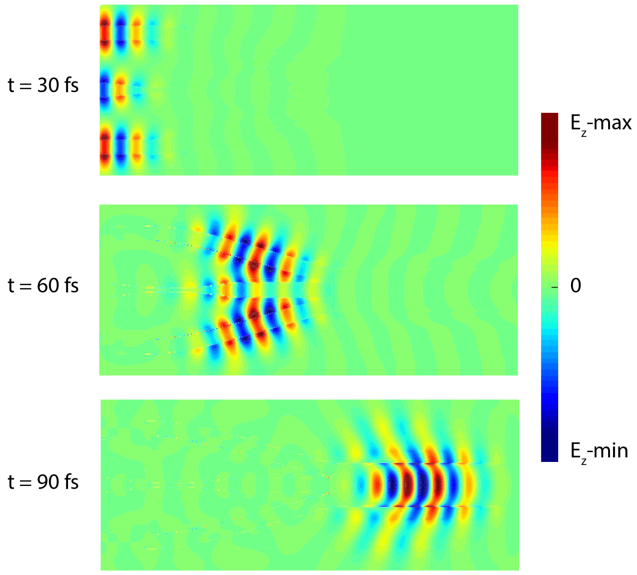
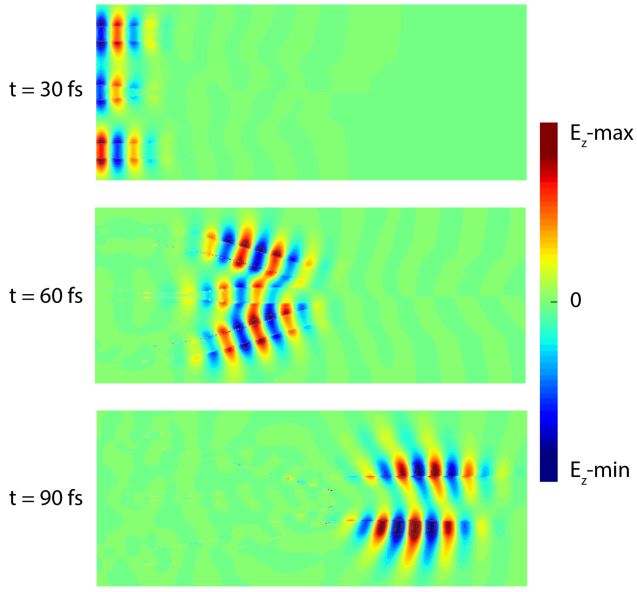


FIG. 4. Cross-section along the xy-plane of the MAJ gate design. The buffer is also displayed below the cross-section for clarity.

In principle the simulated MAJ gate is functional if the output group state separation Δ_{state} is larger than zero. However, for detection in real devices, the separation Δ_{state} should be sufficiently large to allow the detector to distinguish between '1's and '0's. As a first estimation, this separation Δ_{state} should be equal or larger than the amplitude of the input SPP wave packets. A cross-section in the xy-plane of the proposed MAJ gate design is depicted in Figure 4. The dimensions of this configuration are W = 5.5 μm, L = 14 μm and the distance between two input waveguides was chosen 0.5 μm to avoid crosstalk between the E_y-fields in aligning input waveguides. The SPP wave packet originating from the central input 2 is temporarily confined causing a reduction of the total electric field before and after the taper of 57%. Decreasing the amplitude of the central input compensates for the energy losses along the bends from inputs 1 and 3. The output waveguide is two times wider



(a)



(b)

FIG. 5. Time lapses logic operation, (a) Time lapse 111, (b) Time lapse 011.

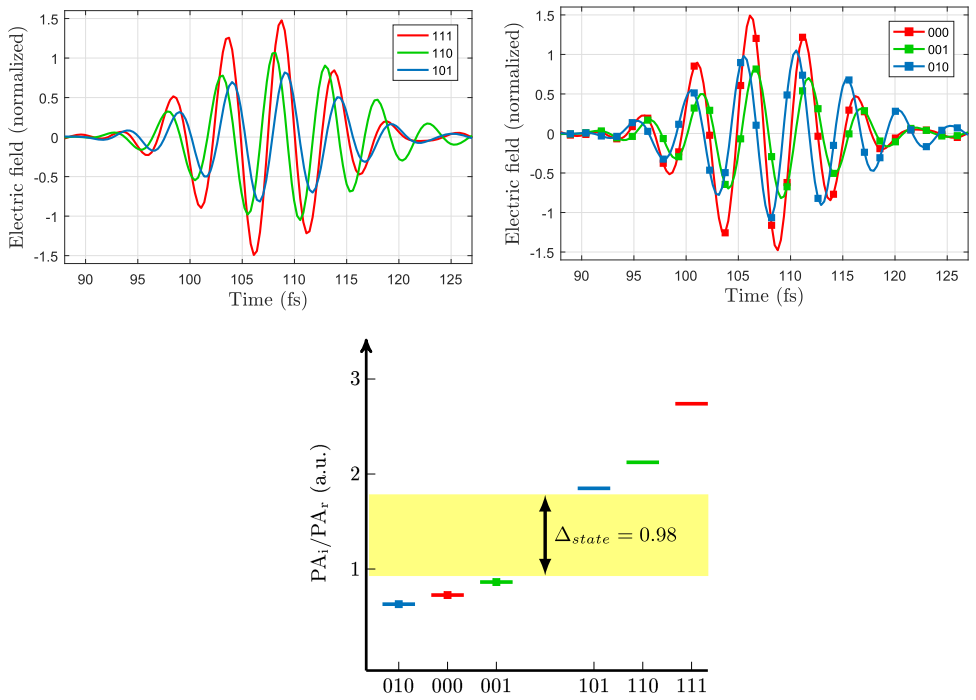


FIG. 6. Output characterization of MAJ gate, (a) Normalized electric field at output with inputs for 1, (b) Normalized electric field at output with inputs for 0, (c) Output state diagram.

then the input waveguides for efficient input to output mode excitation. The tapered regions and the narrow waveguide in between are both 1.5 μm long and the small section is four times narrower than the input waveguides.

The proposed MAJ gate design was tested for functionality by applying all different input combinations and measuring the phase at the output. For two input combinations (111 and 110), a time lapse of the electric field amplitude inside the MAJ gate design is given in Figure 5. The wave computing principle is illustrated here: (t = 30fs) the inputs are excited separately in each input waveguide, (t = 60fs) the SPP wave packets interfere at the waveguide junction and (t = 90fs) propagate towards the output waveguide. The output mode profiles for input combinations 111 and 011 are different due to asymmetry of the 011 input combination. Specific interference based computing architectures can exploit this since more information is carried in the output signal.

The electric field (normalized to the maximum electric field from the source) at the output for different input combinations of the MAJ gate design is shown in Figures 6a and 6b. With these figures, the phase difference for outputs resulting from input combinations 111, 110, 101 and outputs resulting from 000, 001 and 010 can be visually compared. Outputs resulting from input combinations 011 and 100 are identical with 110 and 001 by symmetry, therefore omitted for clarity. Quantitative comparison can be done by employing the introduced figure of merit from Equation (1). The difference in figure of merit between state 101 and 001 was defined in Equation (2) and is $\Delta_{state} = 0.98$ for the proposed design. This can be illustrated by plotting the FOM for all input combinations and is shown in Figure 6c. Keeping in mind this number is normalized by the peak amplitude of the reference signal (Eq. (1)), the state separation is approximately equal to the amplitude of the reference signal. And since the amplitude of the reference signal corresponds to the amplitude of an excited input wave packet, this separation should provide enough margin for distinguishing between '1's and '0's at the output.

In conclusion, in this paper a plasmonic MAJ gate design is proposed and the output state separation Δ_{state} was defined and extracted from simulations. For this design, wave computing relies on interference between different plasmonic modes, which may result in complex mode profiles. These resulting mode profiles can, however, be exploited in specific interference based computing architectures.

The dimensions of the design where chosen to support a long-range plasmonic mode which doesn't decay significantly during propagation in the logic gate input and output waveguides. In this way the SPP interference could be observed in actual simulations, without additional propagation losses, resulting purely from the SPP propagation in the input and output waveguides. However, the proposed design can be scaled beyond the diffraction limit while maintaining the MAJ function. Implementing plasmonic logic gates beyond the diffraction limit has already been demonstrated for multiple logic gates.[14] For even further downscaling, other geometries such as MIM waveguides need to be considered. These provide stronger confinement, resulting in less crosstalk and thus allow denser packing of adjacent MAJ gates. Future research could include simulations of the interference between the output signal and reference signal. Also, it can be examined how reflections and static surface plasmon modes at the waveguide junctions affect the functionality of the MAJ gate. Alternatively, besides exploiting the input dependent output mode profiles, tailored waveguide geometries or dedicated devices can be developed which ensure propagating wave packets are coherent before and after the interference region.

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