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On the electrostatic control achieved in transistors based on multilayered MoS_2: A first-principles study

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In this work, the electrostatic control in metal-oxide-semiconductor field-effect transistors based on MoS_2 is studied, with respect to the number of MoS_2 layers in the channel and to the equivalent oxide thickness of the gate dielectric, using first-principles calculations combined with a quantum transport formalism. Our simulations show that a compromise exists between the drive current and the electrostatic control on the channel. When increasing the number of MoS_2 layers, a degradation of the device performances in terms of subthreshold swing and OFF currents arises due to the screening of the MoS_2 layers constituting the transistor channel. *Published by AIP Publishing.*
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I. INTRODUCTION

Over the last few decades, the scaling of the physical dimensions of metal-oxide-semiconductor field-effect transistors (MOSFETs) has enabled a tremendous increase in computational power following Moore's law.[1] However, recent years have seen an increasing number of issues that have led to performance degradations and to a rise in power consumption. While transistors have been made of silicon for more than five decades, it is believed that this material is reaching its limits for aggressively scaled devices due to a combination of short-channel effects and channel thinning problems, among which are source-to-drain tunneling, gate leakage, and quantum confinement.[2,3] Therefore, alternative materials are being studied to replace Si in the transistor channel. Among the potential candidates, two-dimensional (2D) materials[4] are considered as being "wonder-materials" that would allow further scaling of the transistor physical dimensions down to the atomic scale.[5] Due to their two-dimensional nature, they are expected not to be affected by the channel thinning problem, which arises in silicon and more generally in bulk materials. Although graphene can show an electron mobility of more than 200 000 $cm^2\ V^{-1}\ s^{-1}$,[6] its incorporation in the channel of MOSFETs suffers from the absence of a band gap. Recently, transition metal dichalcogenides (TMDs) have appeared as suitable materials for transistor applications, including MOSFETs[7,8] and alternative devices, such as tunnel field-effect transistors (TFETs),[9] using the advantages of stacking two-dimensional materials.[10] However, the reported drive current remains low and needs to be improved, especially for aggressively scaled devices.[11] To properly understand the behavior of such devices, which consist of multilayered materials, the study of the impact of the number of layers and the dielectric environment on the device switching is crucial, in terms of subthreshold swing (SS) and drive current (I_d). In this work, we investigate the impact of the MoS_2 channel thickness and equivalent oxide thickness (EOT) of the gate dielectric on the performances of single-gated (SG) and double-gated (DG) MOSFETs. The drive current and SS are computed using the Non-Equilibrium Green's Functions (NEGFs) formalism, with a device Hamiltonian built from first-principles calculations, subsequently transformed into Wannier functions.[12]

II. METHODOLOGY

We used the density functional theory (DFT)[13] with the optb86b exchange-correlation functional introduced by Klimeš *et al.* for van der Waals materials[14] and its implementation in the Quantum Espresso software package[15] to compute the electronic band structure of MoS_2 for a number of layers varying from one to four. The carrier effective masses were then evaluated by fitting the valence and conduction bands in the proximity of the band extrema. The phonon mode frequencies and polarization charges were also computed to evaluate the dielectric tensor for each configuration using the density functional perturbation theory (DFPT). The cutoff value for the kinetic energy was set to be 60 Ry, with a k-point density of 0.1 $Å^{-1}$ ($18 \times 18 \times 1$ Monkhorst-Pack grid[16]), which ensures that the total energy is converged within 0.002 eV/atom and that the total forces are inferior to 0.005 eV/Å, using Garrity-Bennett-Rabe-Vanderbilt (GBRV) Ultrasoft pseudopotentials.[17] The Bloch functions obtained from DFT were then transformed into Maximally Localized Wannier Functions (MLWF),[18] using the Wannier90 software package.[19] This process allows building a tight-binding-like Hamiltonian for each configuration, taking into account the interactions up to the sixth nearest neighbor. The transport properties were then computed using the NEGF formalism in the ballistic regime, as implemented in the OMEN software.[20] To obtain a device

Hamiltonian compatible with the quantum transport solver, a rectangular supercell was built from the hexagonal unit cell to simulate the device properties and interactions.

In this work, we studied n-MOSFETs made of a MoS_2 channel, controlled by one or two gates separated from the channel by an insulating material with a high dielectric constant κ_{ox}. The gate length is set to be $L_G = 10$ nm to avoid an intra-band source-to-drain tunneling contribution to the drive current.[21] The gate dielectric has an EOT of 2 nm, 0.5 nm, or 0.1 nm, as shown in Figure 1(a). In the case of a single-gated device, an additional dielectric region equivalent to 20 nm of silicon oxide is defined below the channel, in the opposite side from the gate. The dielectric interface was modeled as being abrupt, i.e., that a direct transition occurs between the different dielectric constants of each region. These later are defined as follows when going (from bottom to top) along the vertical direction of the double gate device: the bottom gate (with a dielectric constant equal to infinity due to its metallic nature), the bottom gate dielectric (dielectric constant labelled as κ_{ox}), the channel (dielectric constant κ_{MoS_2}), the top gate dielectric (dielectric constant κ_{ox}), and the top gate (metallic), as can be seen in Figure 1. The channel is made of 1, 2, 3, or 4 monolayers (MLs) of MoS_2. The doping concentration in the electrodes is set to be 1×10^{13} e/cm^2 (n-type), a value close to the doping concentration achieved experimentally,[22] and the drain-to-source V_{DS} bias is set to be 0.1 V to avoid artifacts due to the ballistic transport calculation, which results in an artificial negative differential resistance if V_{DS} exceeds 0.3 V, as explained by Szabo and coworkers in Ref. 7. The source and drain both have a length of 10 nm. For each configuration, the transmission spectra and drive current-gate voltage characteristics are computed. In order to compare the drive currents of different devices, the current is calculated as a function of the gate overdrive $(V_G - V_T)$, which ranges from -0.5 V to 0.3 V, by steps of 0.05 V. The threshold voltage V_T is evaluated by an extrapolation of the current-voltage curve in the linear regime.

III. RESULTS

A. Electronic properties

The energy band structures are computed for one to four monolayers of MoS_2, along the symmetry point path K-Γ-M-K′. In Figure 2, the band structures computed in DFT are shown as well as the one obtained after a projection on a Wannier basis. They are perfectly overlapping in our calculations. In the monolayer case, the band gap is found to be direct at the K symmetry point and to be about 1.81 eV, which is in agreement with experimental measurements.[23] An increase in the number of MoS_2 layers changes the band positions and the gap becomes indirect, the top of the valence band (TVB) being shifted to Γ and the bottom of the conduction band (BCB) being located along the Γ-K symmetry line, where a band splitting occurs. As expected from this generalized gradient approximation (GGA) type of exchange-correlation functional, the bulk band gap (1.2 eV) is underestimated in our calculations (0.75 eV).[24] Nevertheless, qualitatively speaking, the trends observed when increasing the number of layers are in agreement with experimental results.[23] From 1 to 2 MLs, both the electron and hole effective masses (m_e^* and m_h^*, respectively) increase, as indicated in Table I. The increase in m_e^* from $0.45\,m_0$ to $0.59\,m_0$ hints at a possible reduction in the drive current in the n-MOSFET. Beyond 2 MLs, the effective masses converge towards the bulk values, with results similar to previously reported simulations.[25] It should also be noticed that for multi-layered MoS_2, the electron effective mass becomes anisotropic. In the device simulations, we chose the direction with the lowest effective mass as being the transport one.

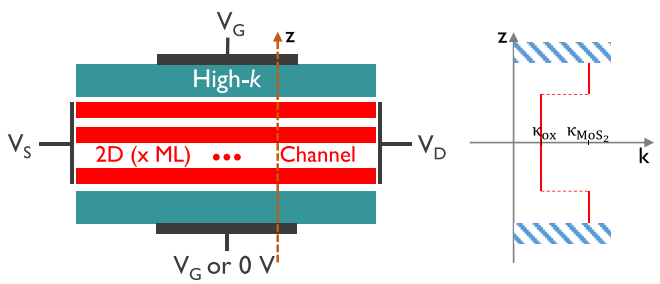

FIG. 1. (a) Schematic view of the MOSFET configuration considered in this work. The device consists of a channel (red) made of MoS_2, contacted with doped source and drain regions, where potentials V_S and V_D are applied, respectively. The device is controlled by one or two gates, with a gate voltage V_G. The gates are separated from the channel by a high-κ material. (b) Dielectric profile in the device along z, the out-of-plane (vertical) axis.

The dielectric constant calculations show a raise in the dielectric tensor components when the number of monolayers increases, though this increase is much lower than the one in the physical thickness (see Table I). As a result, the equivalent oxide thickness of the channel, which indicates how the channel will screen the gate control, grows steadily with the number of MoS_2 monolayers. The computed dielectric constants for the monolayer and bulk cases agree with the previous DFT-local density approximation (LDA) results by Molina-Sánchez and Wirtz,[26] and the component in the direction in which the gate bias is applied (perpendicular to the layers) is smaller than the $11.8 \times \epsilon_0$ found in silicon.

B. Drive current-gate voltage characteristics

Based on the results discussed above, a change in the device behavior is expected upon an increase in the number of MoS_2 monolayers. We first computed the drive current-gate voltage (I-V) curves for a double-gated (DG) device with a gate dielectric EOT value of 2 nm, a bias voltage V_{DS} fixed at 0.1 V, and a doping concentration of 10^{13} e/cm^2. The results, presented in Figure 3 in both linear and logarithmic scales, show that the drive current density at $V_G - V_T = 0.2$ V, denoted by I_d, ranges from 300 μA/μm to 550 μA/μm and varies with the number of layers. From one to three monolayers, the drive current is increased by around 35%. However, at 4 MLs, it drops to values even inferior by 28% compared with the one reported in the monolayer case. There is almost no increase in current going from 1 ML to 2 MLs, due to the fact that the benefit of the second layer is counterbalanced by the increase in the electron effective mass in the channel, from $0.45\,m_0$ to $0.59\,m_0$ (cf. Table I). The origin of the drop in current above 3 MLs can be found in the electrostatic control from the gate on the channel. Due to the increase in its physical thickness, which is not counterbalanced by a similar increase in its dielectric constant, the electrostatic control is progressively lost, which is reflected by

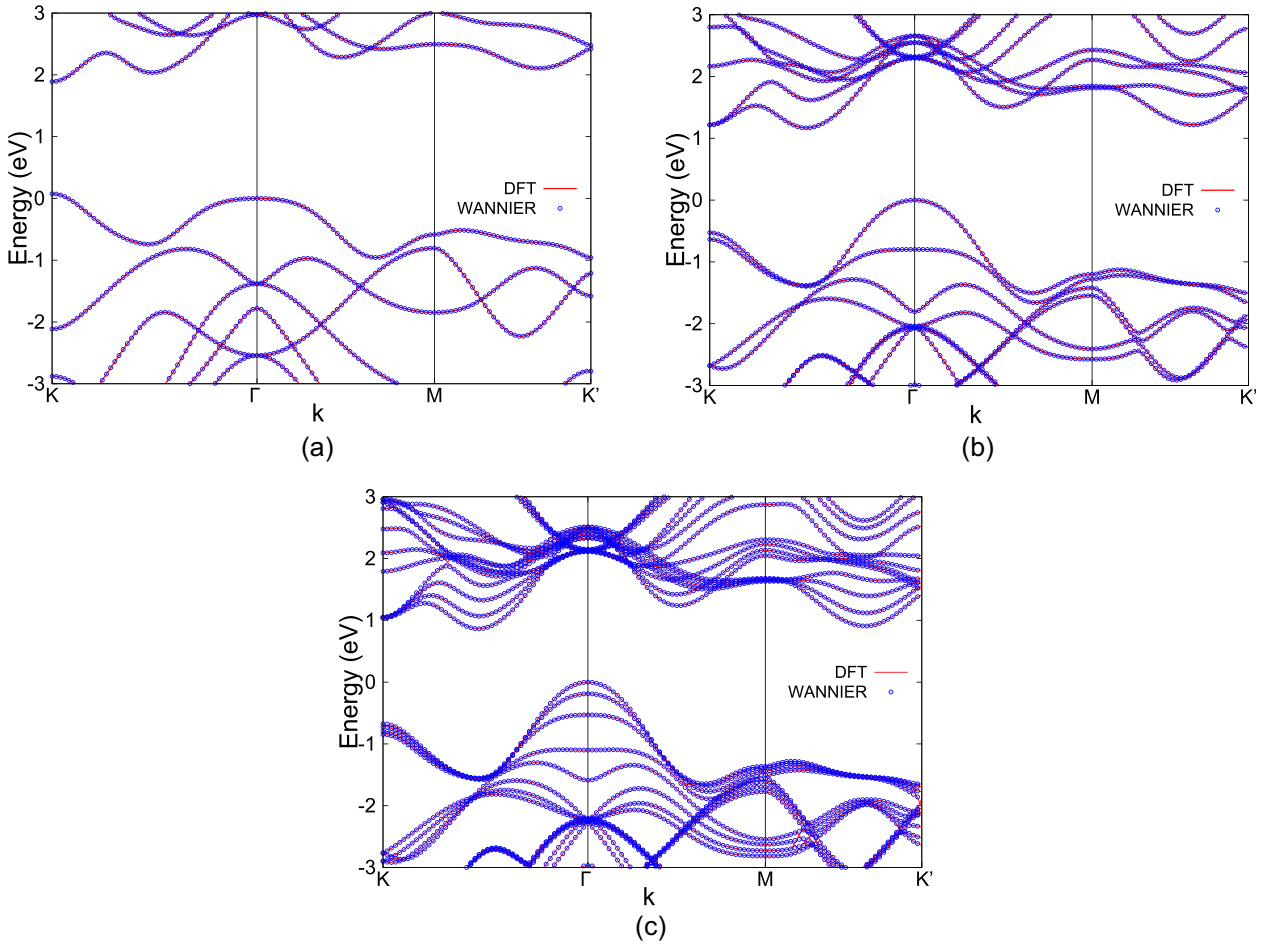

FIG. 2. Band structures of isolated molybdenum disulfide in vacuum with (a) a single layer, (b) two layers, and (c) four layers. The solid line shows the band structure computed at the DFT level. The circles show the band structure obtained after the projection of the Bloch states on a Wannier basis.

an increase in both OFF current I_{OFF} and the subthreshold swing (SS), as can be seen in Figure 3(b). As the number of monolayers increases, the subthreshold swing is degraded, from 69 mV/dec for a single monolayer to 87 mV/dec for four monolayers. Mishra *et al*. have theoretically shown a degradation due to a large density of states in ultrashort channel MoS_2 transistors,[27] while Kang *et al*. experimentally demonstrated an increase in the current with the number of MoS_2 layers followed by a degradation due to the fact that the metal contact fails to connect to all the layers.[28]

Here, we identify an important additional contribution to this degradation, which comes from the dielectric screening of the MoS_2 channel, linked to the component of the dielectric tensor along the direction normal to the layers.

A reduction in the EOT of the gate oxide should improve the switching of the MOSFET, by reducing I_{OFF} and the subthreshold swing. Note that the values lower than 0.5 nm have been reported recently.[29] So we considered a hypothetic value of 0.1 nm to investigate the best achievable behavior in our

TABLE I. Evolution of the electronic properties of MoS_2 as a function of the number of layers, computed at the DFT-optb86b level. In the effective mass columns, m_0 is the electron rest mass and the superscript indicates the location of the band extrema: (a) K, (b) between K and Γ, and (c) Γ. The components of the dielectric tensor ϵ_{xx}, ϵ_{yy}, and ϵ_{zz} are presented as well as the MoS_2 thickness from the top and bottom atoms. The equivalent oxide thickness of the channel, t_{equiv}, is computed by using the out-of-the-plane component of the dielectric tensor to reveal its dielectric screening.

		Electron effective mass ($\times m_0$)		Hole effective mass ($\times m_0$)		Dielectric constant in-plane and out-of-plane ($\times \epsilon_0$)			
Number of MoS_2 layers	Band gap (eV)	Longitudinal	Transversal	Longitudinal	Transversal	$\epsilon_{xx} = \epsilon_{yy}$	ϵ_{zz}	Thickness (nm)	Channel equivalent oxide thickness $t_{equiv} = t_{channel} \frac{\epsilon_{channel}}{\epsilon_{SiO_2}}$ (nm)
1	1.81	0.45[a]	0.45[a]	0.56[a]	0.56[a]	5.21	1.35	0.3	0.9
2	1.23	0.59[b]	0.81[b]	0.95[c]	0.95[c]	6.74	1.53	0.9	2.3
3	0.97	0.58[b]	0.78[b]	0.73[c]	0.73[c]	9.63	2.07	1.5	2.8
4	0.88	0.57[b]	0.75[b]	0.66[c]	0.66[c]	10.96	2.45	2.1	3.3
Bulk	0.74	0.55[b]	0.73[b]	0.59[c]	0.59[c]	15.57	7.27	∞	/

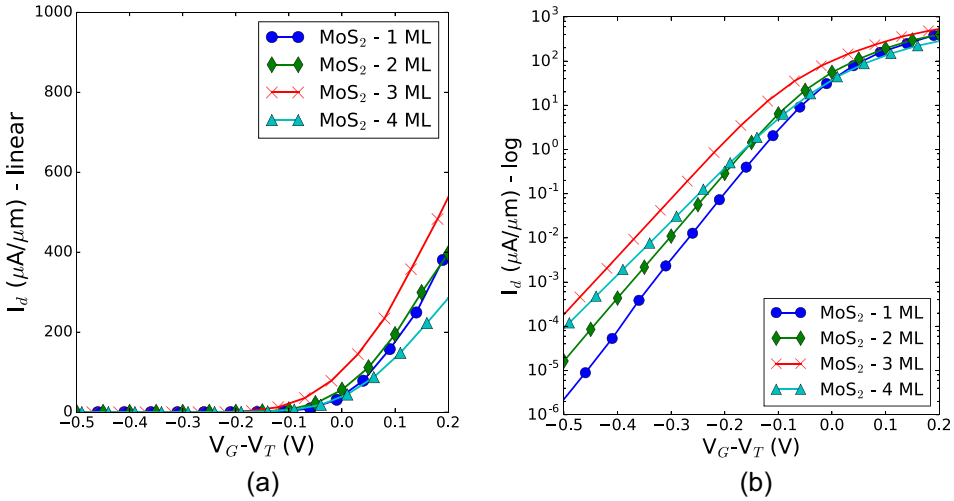

FIG. 3. Current-overdrive voltage curves for double-gated MoS_2 n-MOSFETs in linear (left) and logarithmic scales (right). The curves are colored in blue for a single monolayer (ML), green for 2 MLs, red for 3 MLs, and turquoise for 4 MLs.

double-gated device models. In a double-gated device, the subthreshold swing can be reduced to values close to the case of an ideal MOSFET at room temperature (60 mV/dec).[30] For instance, in the configuration displaying the highest drive current, i.e., for the MOSFET built from a tri-layered MoS_2, the SS was reduced from 79 mV/dec (EOT = 2 nm) to 67 mV/dec (EOT = 0.5 nm) and down to 61 mV/dec (EOT = 0.1 nm), as shown in Figure 4. Even with an aggressive EOT of 0.5 nm, equivalent to about 3 nm of HfO_2, the subthreshold swing remains degraded, with a value of 67 mV/dec for 3 MLs and 69 mV/dec for 4 MLs (see Table II), underlining the fact that the dielectric screening of MoS_2 plays the most important role. This phenomenon is illustrated in Figure 5 by plotting the subthreshold swing values versus the computed EOT of the channel material. There is therefore a compromise between the amplitude of the drive current and the electrostatic control on the device as revealed by the subthreshold swing.

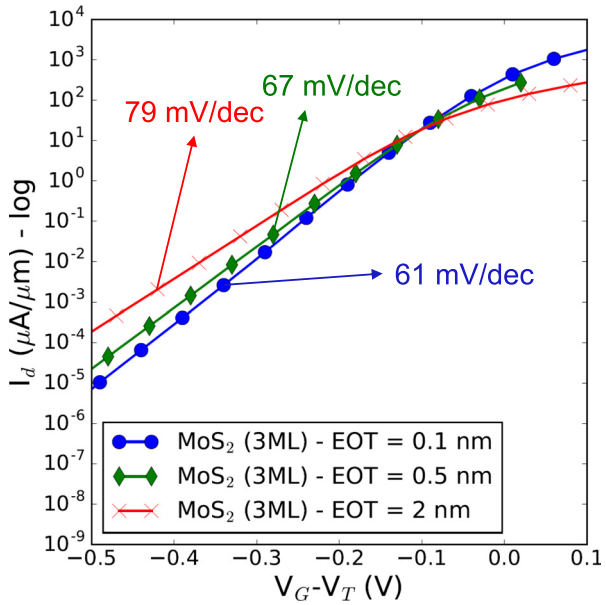

FIG. 4. Current-overdrive gate voltage characteristics for a double-gated MOSFET based on tri-layered MoS_2 for an effective oxide thickness ranging from 0.1 nm to 2 nm. The subthreshold swing values are indicated by the colored arrows.

We also studied single-gated (SG) MOSFETs, which are easier to fabricate. In this case, the performance degradation is even stronger, with SS values that range from 87 mV/dec to 131 mV/dec (see Figure 6 and Table II). Even with a very aggressive EOT of 0.1 nm, a loss in electrostatic control can be seen for a channel thickness of 3 MLs and 4 MLs, with the best SS values always exceeding 70 mV/dec (with 72 mV/dec and 73 mV/dec, respectively), as the MoS_2 screening is enforced by the absence of a second gate.

To confirm this screening phenomenon, we also performed simulations of the single-gated devices with a gate

TABLE II. Subthreshold swing in double-gated and single-gated MoS_2 n-MOSFETs and dependence with respect to the number of MoS_2 monolayers and to the EOT of the gate oxide(s).

Device type	Double-gated			Single-gated		
	EOT (nm)			EOT (nm)		
Number of layers	0.1	0.5	2	0.1	0.5	2
1	60.4	63.2	69.4	62.5	67.8	87.1
2	60.2	64.2	74.0	63.5	72.7	99.2
3	61.2	66.6	78.6	72.4	79.1	107.7
4	62.4	69.5	87.4	73.0	86.5	131.5

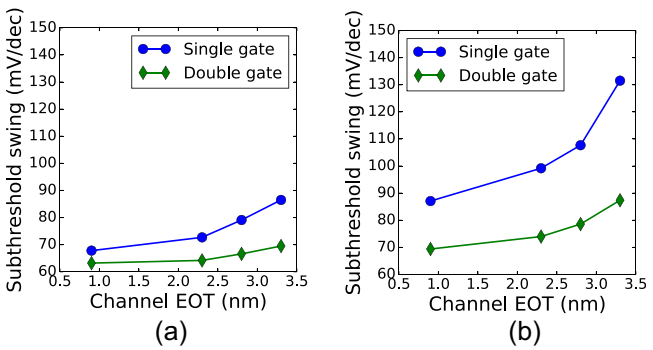

FIG. 5. Evolution of the subthreshold swing with respect to the computed equivalent oxide thickness of the MoS_2 channel for an effective oxide thickness of the gate dielectric of (a) 0.5 nm and (b) 2 nm. The circles show the results for single-gated devices while diamonds show the results for double-gated ones.

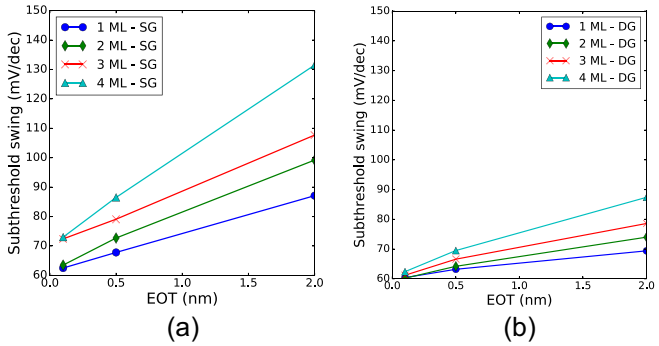

FIG. 6. Evolution of the subthreshold swing with respect to the EOT in (a) single-gated and (b) double-gated MoS_2 MOSFETs.

oxide EOT of 0.1 nm and a "fictitious" MoS_2 channel for which the dielectric constant is artificially increased to be $\kappa = 20 \times \epsilon_0$. Although the channel material is not representative of a real MoS_2, this approach allows probing the impact of the dielectric screening of the channel body on the device operation. The I_d vs. V_G-V_T characteristics for a single gated MoS_2 (3 MLs) nMOSFET are shown in Figure 7. This artificially enhanced dielectric constant improves the electrostatic control achieved by reducing the screening within the MoS_2 layers. This is translated into a lower OFF current and higher a drive one beyond the threshold voltage. In this configuration, the computed SS for 3 MLs and 4 MLs are, respectively, 68 and 70 mV/dec (against 70 and 73 mV/dec in the "real" MoS_2), demonstrating the importance of the dielectric constant of the channel on the electrostatic control achieved in 2D-based MOSFETs.

IV. CONCLUSIONS

The impact of the channel thickness and equivalent oxide thickness of the gate dielectric on the performances of single- and double-gated MoS_2-based MOSFETs has been theoretically studied. An increase in the number of MoS_2 layers up to three is predicted to improve the drive current, however, at the expense of a loss in the electrostatic control. This is due to the low dielectric constant of MoS_2 and resulting screening of the channel by the MoS_2 layers. Consequently, the use of two-dimensional materials with a higher permittivity than MoS_2 may help improving the device characteristics, together with an aggressive EOT scaling.

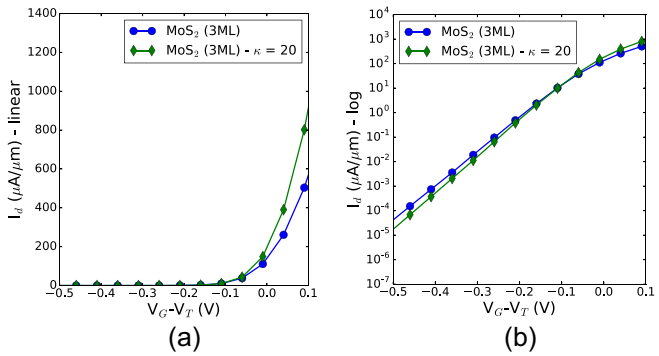

FIG. 7. Impact of the dielectric constant on the current-overdrive voltage curves for a single-gated MoS_2 n-MOSFETs in linear (left) and logarithmic scale (right). The filled circles show the curve for MoS_2 (3 MLs) with a gate oxide EOT of 0.1 nm. The filled diamonds show the same device but with a dielectric constant of MoS_2 tuned to be $\kappa = 20 \times \epsilon_0$.

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[1]G. E. Moore, "Cramming more components onto integrated circuits," Electronics **38**, 114–117 (1965), see http://dx.doi.org/10.1109/jproc.1998.658762.
[2]M. Luisier, M. Lundstrom, D. A. Antoniadis, and J. Bokor, "Ultimate device scaling: Intrinsic performance comparisons of carbon-based, InGaAs, and Si field-effect transistors for 5 nm gate length," in Electron Devices Meeting (IEDM), Washington, DC, 2011.
[3]M. Leong, B. Doris, J. Kedzierski, and Y. Min, "Silicon device scaling to the sub-10-nm regime," Science **306**(5704), 2057–2060 (2004).
[4]K. S. Novoselov, A. K. Geim, S. V. Morozov, D. Jiang, Y. Zhang, S. V. Dubonos, I. V. Grigorieva, and A. A. Firsov, "Electric field effect in atomically thin carbon films," Science **306**, 666 (2004).
[5]F. Schwierz, J. Pezoldt, and R. Granzner, "Two-dimensional materials and their prospects in transistor electronics," Nanoscale **7**, 8261 (2015).
[6]K. I. Bolotin, K. J. Sikes, Z. Jiang, M. Klima, G. Fudenberg, J. Hone, P. Kim, and H. L. Stormer, "Ultrahigh electron mobility in suspended graphene," Solid State Commun. **146**, 351–355 (2008).
[7]A. Szabo, R. Rhyner, and M. Luisier, "*Ab initio* simulation of single- and few-layer MoS_2 transistors: Effect of electron-phonon scattering," Phys. Rev. B **92**, 035435 (2015).
[8]B. Radisavljevic, A. Radenovic, J. Brivio, V. Giacometti, and A. Kis, "Single-layer MoS_2 transistors," Nat. Nanotechnol. **6**, 147–150 (2011).
[9]A. Szabo, S. J. Koester, and M. Luisier, "Metal-dichalcogenide hetero-TFETs: Are they a viable option for low power electronics?," in 72nd Annual Device Research Conference (DRC), Santa Barbara, 2014.
[10]A. K. Geim and I. V. Grigorieva, "Van der Waals heterostructures," Nature **499**, 419 (2013).
[11]Y. Liu, J. Guo, Y. Wu, E. Zhu, N. O. Weiss, Q. He, H. Wu, H.-C. Cheng, Y. Xu, I. Shakir, Y. Huang, and X. Duan, "Pushing the performance limit of sub-100 nm molybdenum disulfide transistors," Nano Lett. **16**, 6337–6342 (2016).
[12]G. H. Wannier, "Dynamics of band electrons in electric and magnetic fields," Rev. Mod. Phys. **34**(4), 645–654 (1962).
[13]W. Kohn and L. J. Sham, "Self-consistent equations including exchange and correlation effects," Phys. Rev. **140**, A1133 (1965).
[14]J. Klimeš, D. R. Bowler, and A. Michaelides, "Van der Waals density functionals applied to solids," Phys. Rev. B **83**, 195131 (2011).
[15]P. Giannozzi, S. Baroni, N. Bonini, M. Calandra, R. Car, C. Cavazzoni, D. Ceresoli, G. L. Chiarotti, M. Cococcioni, I. Dabo, A. Dal Corso, S. de Gironcoli, S. Fabris, G. Fratesi, R. Gebauer, U. Gerstmann, C. Gougoussis, A. Kokalj, M. Lazzeri, L. Martin-Samos, N. Marzari, F. Mauri, R. Mazzarello, S. Paolini, A. Pasquarello, L. Paulatto, C. Sbraccia, S. Scandolo, G. Sclauzero, A. P. Seitsonen, A. Smogunov, P. Umari, and R. M. Wentzcovitch, "QUANTUM ESPRESSO: A modular and open-source software project for quantum simulations of materials," J. Phys.: Condens. Matter **21**, 395502 (2009).
[16]H. J. Monkhorst and J. D. Pack, "Special points for Brillouin-zone integrations," Phys. Rev. B **13**, 5188 (1976).
[17]K. F. Garrity, J. W. Bennett, K. M. Rabe, and D. Vanderbilt, "Pseudopotentials for high-throughput DFT calculations," Comput. Mater. Sci. **81**, 446–452 (2014).
[18]N. Marzari and D. Vanderbilt, "Maximally localized generalized Wannier functions for composite energy bands," Phys. Rev. B **56**, 12847 (1997).
[19]A. A. Mostofi, J. R. Yates, G. Pizzi, Y.-S. Lee, I. Souza, D. Vanderbilt, and N. Marzari, "An updated version of wannier90: A tool for obtaining maximally-localised Wannier functions," Comput. Phys. Commun. **185**(8), 2309–2310 (2014).
[20]M. Luisier and G. Klimeck, "OMEN an atomistic and full-band quantum transport simulator for post-CMOS nanodevices," in 8th IEEE Conference on Nanotechnology, 2008.
[21]A. K. A. Lu, G. Pourtois, T. Agarwal, A. Afzalian, I. P. Radu, and M. Houssa, "Origin of the performances degradation of two-dimensional-

based metal-oxide-semiconductor field effect transistors in the sub-10 nm regime: A first-principles study," Appl. Phys. Lett. **108**, 043504 (2016).
[22]A. Tarasov, S. Zhang, M.-Y. Tsai, P. M. Campbell, S. Graham, S. Barlow, S. R. Marder, and E. M. Vogel, "Controlled doping of large-area trilayer MoS_2 with molecular reductants and oxidants," Adv. Mater. **27**, 1175–1181 (2015).
[23]K. F. Mak, C. Lee, J. Hone, J. Shan, and T. F. Heinz, "Atomically thin MoS_2: A new direct-gap semiconductor," Phys. Rev. Lett. **105**, 136805 (2010).
[24]K. K. Kam and B. A. Parkinson, "Detailed photocurrent spectroscopy of the semiconducting group VI transition metal dichalcogenides," J. Phys. Chem. **86**, 463–467 (1982).
[25]M. Houssa, A. Dimoulas, and A. Molle, "Theoretical study of transition metal dichalcogenides," in *2D Materials for Nanoelectronics* (CRC Press, 2016), pp. 150–151.
[26]A. Molina-Sánchez and L. Wirtz, "Phonons in single-layer and few-layer MoS_2 and WS_2," Phys. Rev. B **84**, 155413 (2011).
[27]V. Mishra, S. Smith, L. Liu, F. Zahid, Y. Zhu, H. Guo, and S. Salahuddin, "Screening in ultrashort (5 nm) channel MoS_2 transistors: A full-band quantum transport study," IEEE Trans. Electron Devices **62**(8), 2457–2463 (2015).
[28]J. Kang, W. Liu, and K. Benerjee, "High-performance MoS_2 transistors with low-resistance molybdenum contacts," Appl. Phys. Lett. **104**, 093106 (2014).
[29]J.-H. Ahn and S.-H. Kwon, "Sub-0.5 nm equivalent oxide thickness scaling for Si-doped $Zr_{1-x}Hf_xO_2$ thin film without using noble metal electrode," ACS Appl. Mater. Interfaces **7**, 15587–15592 (2015).
[30]S. Datta, *Quantum Transport: Atom to Transistor* (Cambridge University Press, 2013).