Manuscript Details

Manuscript number	MATERIALSCHAR_2019_3231_R1
Title	TEM investigation of the role of the polycrystalline-silicon film/substrate interface in high quality radio frequency silicon substrates
Article type	Research Paper

Abstract

The microstructural characteristics of two polycrystalline silicon (poly-Si) films with different electrical properties produced by low-pressure chemical vapour deposition on top of high resistivity silicon substrates were investigated by advanced transmission electron microscopy (TEM), including high resolution aberration corrected TEM and automated crystallographic orientation mapping in TEM. The results reveal that the nature of the poly-Si film/Si substrate interface is the main factor controlling the electrical resistivity of the poly-Si films. The high resistivity and high electrical linearity of poly-Si films are strongly promoted by the ∑3 twin type character of the poly-Si/Si substrate interface, leading to the generation of a huge amount of extended defects including stacking faults, ∑3 twin boundaries as well as ∑9 grain boundaries at this interface. Furthermore, a high density of interfacial dislocations has been observed at numerous common and more exotic grain boundaries deviating from their standard crystallographic planes. In contrast, poly-Si film/Si substrate interfaces with random character do not favour the formation of such complex patterns of defects, leading to poor electrical resistivity of the poly-Si film. This finding opens windows for the development of high resistivity silicon substrates for Radio Frequency (RF) integrated circuits (ICs) applications.

Keywords	polycrystalline silicon; Transmission electron microscopy; Grain boundaries

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UCLouvain

Université catholique de Louvain
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Dr. Lipeng DING

Dear Editors,

We would like to resubmit our revised manuscript entitled "**TEM investigation of the role of the polycrystalline-silicon film/substrate interface in high quality radio frequency silicon substrates**" by Lipeng Ding, Jean-Pierre Raskin, Gunnar Lumbeeck, Dominique Schryvers and Hosni Idrissi to **Materials Characterization** for publication.

First of all, we greatly thank the editor's careful treatment and kind consideration on our manuscript, and also the reviewer's thorough review and valuable comments. In the revised manuscript, we really take care of all suggestions and comments given by the editor and the reviewers during modifying the manuscript.

All the changes have been highlighted in red color in the revised manuscript.

Sincerely Yours

Lipeng DING

Corresponding author (on behalf the other authors)

First of all, we appreciate the reviewers' thorough review and valuable comments. Our responses to the reviewers' suggestions and comments are listed below.

Reviewer #1

The authors have performed beautiful TEM characterizations on grain boundaries and related defects in poly-Si film grown on high resistivity Si for RF applications. The electrical resistivity has been found to be determined mainly by the interface defects. The results presented are interesting and can be accepted after minor revision. There are several questions and comments listed as the following,

1. ***Why the same CVD process resulted in different grain boundaries like sigma 3 dominated or random boundary at the interface?***

The present study clearly demonstrates that the nature of the poly-Si film/Si substrate interface is the main factor controlling the electrical resistivity of the poly-Si films. As stated in the main text, the origin of this difference can be attributed to slight difference in surface quality of the Si substrate, in the LPCVD parameters or to the presence of impurities at the interface. This question is very relevant but will require further investigations, which goes beyond the scope of the present work. However, such phenomenon should be seriously considered for the development of high resistivity silicon substrates for Radio Frequency (RF) integrated circuits (ICs) applications.

2. ***For the formation of different types of boundaries, is there any effect from Si substrate? For instance, the surface cleaning process or substrate temperature, and how about the effect from different crystal orientation like Si (100) vs. (111)?***

Yes, the surface cleaning process could have an effect on the formation of different types of boundaries at the interface. Some impurities present at the Si substrate surface could also influence the nature of the boundaries formed at the interface while the substrate temperature could affect the fraction of grain boundaries at the interface. The different crystal orientation like Si(100) vs.(110) could also influence the nature of grain boundaries. For example, the $(100)_{\text{Si substrate}}$ plane leads to the formation of high angle grain boundary with $(110)_{\text{film}}$ plane. The $(100)_{\text{Si substrate}}$ plane forms $\sum 5$GB or $\sum 13a$GB with $(100)_{\text{film}}$ plane, while $(110)_{\text{Si substrate}}$ plane leads to the formation of $\sum 3$, $\sum 9$ or $\sum 27$GB with $(110)_{\text{film}}$ plane. In the absence of experimental evidences of such features in the present work, we added the references [12-14] cited above to the main text in order to discuss potential sources of the observed difference.

3. ***Can the author explain in detail about the simulation result based on Atlas, like the different decay rate of resistivity under inversion vs. accumulation? In Fig. 1c, the resistivity under inversion (V_{DC}=4V), why the peak resistivity appears at around a depth of 10 μm?***

The difference of resistivity between inversion (150 mΩ.cm, V_{DC} = 4 V) and accumulation (1.5 Ω.cm, V_{DC} = -4 V) can be explained by (i) the carrier mobility of electrons is approximately 2-3 times larger than holes mobility in silicon, and (ii) the flatband voltage of the sample is at -1.98 V which means that the density of electrons at the interface is much larger than holes at 0 V, the interface is naturally under weak inversion. These two facts explain the lower resistivity (higher conductivity) at the SiO_2-silicon substrate interface when the interface is in

inversion regime. In Fig. 1c, a peak of resistivity appears at around 10 µm depth when the substrate is biased under inversion regime (V_{DC} = 4 V). This peak of resistivity corresponds to the location of the so-called depletion zone. At V_{DC} = 4 V, from the SiO_2-Si interface we have right at the interface a strong inversion, a depletion zone (at around 10 µm) and finally we recover the neutral zone of the substrate, it means the nominal resistivity of the silicon substrate, i.e. 10 kΩ.cm in the simulated case.

4. ***Just one comment, when discuss about the carrier trapping in trap layer, it is not only related with the type of grain boundaries, but also the density of defects at interface.***

True. The following sentence was added in the main text (page 15, paragraph 1) to clarify this point: "it is worth noting that the carrier trapping capacity in trap layer is not only linked to the type of grain boundaries, but also the density of defects at interface [18,19]. A high density of the interfacial defects leads to significant increase of the electrical resistivity of the poly-Si films."

5. ***Would the author comment on the effect from interface between SiO_2 and poly-Si?***

The amorphous SiO_2 film is not expected to play a role in the formation of defects in the poly-Si film because it was deposited after the growth of the poly-Si film. This is in agreement with the fact that, in contrast with the crystal/crystal poly-Si film/Si substrate interface, the amorphous/crystal SiO_2/poly-Si interface is very similar in samples A and B (sse Figure 2). However, the SiO_2/poly-Si interface can still influence the electrical properties of the film because of some dislocations could emit from the amorphous/crystal interface or some oxidation or clusters formed at the interface.

Reviewer # 2

This paper studied the microstructural characteristics of two polycrystalline silicon (poly-Si) films with different electrical properties by advanced transmission electron microscopy (TEM). The results reveal that the nature of the poly-Si film/Si substrate interface is the main factor controlling the electrical resistivity of the poly-Si films. The high resistivity and high electrical linearity of poly-Si films are strongly promoted by the Σ3 twin type character of the poly-Si/Si substrate interface. In contrast, poly-Si film/Si substrate interfaces with random character do not favour the formation of such complex patterns of defects, leading to poor electrical resistivity of the poly-Si film. Two questions, firstly, the three wafer substrates are single crystalline, <111> or <100> orientation? Secondly, interface character is a key factor determining the electrical properties, so how about the mismatch difference between sample A interface and sample B interface? Overall, this work is highly interesting in understanding the intrinsic origin for the effect of interface character on electrical resistivity of the poly-Si films and is suitable for publish in Materials Characterization.

The three wafer substrates are single crystalline with <100> orientation. The sentence "The starting substrates are three monocrystalline high resistivity (HR) Si bulk wafers with <110> orientation and…" was added in the revised manuscript. For the question regarding the mismatch difference between the sample A and sample B interface, one can notice that the poly-Si/Si substrate interface in sample B exhibits a∑3 twin type character alternating between

$\sum 3\{111\}$ CTBs and $\sum 3\{112\}$ incoherent ITBs that can be associated to a small mismatch. In contrast, the same interface in Sample A exhibits a random character leading to a higher mismatch that change with changes of the grains orientation at the interface. This is also in agreement with the strain field observed at the interface of Sample A in Figures 6a and 6b that can be explained by the presence of a high density of dislocations at the interface.

All the changes in the manuscript are highlighted in red color.

Hightlights

- The nature of the poly-Si film/Si substrate interface is the main factor controlling the electrical resistivity of the poly-Si films.
- The ∑3 twin type character of the poly-Si/Si substrate interface and the interaction between different types of interfaces could lead to the generation of a huge amount of extended defects, which significantly improve the electrical resistivity of the poly-Si films.
- poly-Si film/Si substrate interfaces with random character do not favour the formation of high density of interfacial dislocations, leading to poor electrical resistivity of the poly-Si film.

TEM investigation of the role of the polycrystalline-silicon film/substrate interface in high quality radio frequency silicon substrates

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Abstract

The microstructural characteristics of two polycrystalline silicon (poly-Si) films with different electrical properties produced by low-pressure chemical vapour deposition on top of high resistivity silicon substrates were investigated by advanced transmission electron microscopy (TEM), including high resolution aberration corrected TEM and automated crystallographic orientation mapping in TEM. The results reveal that the nature of the poly-Si film/Si substrate interface is the main factor controlling the electrical resistivity of the poly-Si films. The high resistivity and high electrical linearity of poly-Si films are strongly promoted by the ∑3 twin type character of the poly-Si/Si substrate interface, leading to the generation of a huge amount of extended defects including stacking faults, ∑3 twin boundaries as well as ∑9 grain boundaries at this interface. Furthermore, a high density of interfacial dislocations has been observed at numerous common and more exotic grain boundaries deviating from their standard crystallographic planes. In contrast, poly-Si film/Si substrate interfaces with random character do not favour the formation of such complex patterns of defects, leading to poor electrical resistivity of the poly-Si film. This finding opens windows for the development of high resistivity silicon substrates for Radio Frequency (RF) integrated circuits (ICs) applications.

Keywords: polycrystalline silicon; Transmission electron microscopy; Grain boundaries

1. Introduction

Polycrystalline silicon (poly-Si) films are widely used in integrated circuit technology for solar cells [1], thin film transistors [2, 3], piezo-resistance elements for pressure sensors [4], as trapping layer in silicon-based high resistivity substrates for Radio Frequency (RF) integrated

circuits (ICs) [5, 6], and many other applications due to their low cost and high-efficiency [7, 8]. The electrical properties of poly-Si films are strongly influenced by various extended defects such as grain boundaries (GB), twin boundaries (TB) and intra-granular defects. GBs are electrical potential barriers and scattering sites, which can act as recombination centres leading to electrical efficiency loss [9]. These defects can also act as gettering centres for impurity elements and thus significantly decrease the carrier transport mobility [10, 11]. Depending on the foreseen application, the number of electrically active defects must be as low as possible for thin film transistors (TFT) or solar cells for instance, and on the contrary as high as possible in the case of high resistivity silicon substrates for high frequency applications. The poly-Si samples analyzed in the present paper are developed for the latter case as described hereafter.

It is generally argued that the electrical activity of GBs depends on their character. Intense investigations have been performed in the past to reveal the correlation between the character and the electrical activity of GBs [10, 12-14]. For instance, Chen *et al*. found that the GB character has no significant effect on the recombination activity of 'clean' GBs [10]. However, in impurity contaminated GBs, the recombination activity is heavily influenced by the GB character, indicating that this activity is mainly controlled by the gettering ability of GBs. The recombination activity of GBs can be classified as follows: small angle GB (SAGB) > random GB (RGB) > high-∑ GB > low-∑ GB [13]. Because of the low energy, coincidence site lattice (CSL) GBs usually exhibit a lower recombination activity compared with R-GBs. Furthermore, high-∑ GBs (such as ∑9 and ∑27) are more electrically active compared with low-∑ GBs. High-∑ GBs can also act as sites for dislocation nucleation [15, 16]. On the other hand, ∑3 {111} coherent twin boundaries (CTBs) exhibit very low interfacial energy and negligible electrical activity, making them acceptable defects in poly-Si when high mobility electronic transport and low recombination rates are targeted [17].

Both experimental observations and theoretical calculations have shown that the recombination activity of GBs is related to the density of dislocations at the boundary plane [18, 19]. The higher dislocation density in random and high-∑ GBs is thus the main reason for their high recombination activity. Therefore, increasing the proportion of CSL GBs, especially the low-∑ GBs is essential for improving the electrical properties of poly-Si films when high carrier mobility is required like in the case of TFT or solar cells. On the contrary, in the case of trap-rich high resistivity silicon or Silicon-on-Insulator (SOI) substrates, highly concentrated electrically active defects in poly-Si are required. Indeed, as demonstrated in [5, 6] thanks to the introduction of an undoped poly-Si layer characterized by a high density of electrically active traps, the high resistivity properties of the used silicon substrate required for building high quality RF ICs are fully recovered.

In the present study, extensive transmission electron microscopy (TEM) characterizations have been performed in order to investigate poly-Si films produced by low pressure chemical vapour deposition (LPCVD) on top of high resistivity silicon substrates. The results demonstrate a clear correlation between the good high frequency performance in terms of effective resistivity and linearity with the high density of the extended defects confined between the poly-Si film and the silicon substrate.

2. Materials and methods

The starting substrates are three monocrystalline high resistivity (HR) Si bulk wafers with <100> orientation and nominal resistivity specified by the manufacturer as larger than 10000 Ω.cm. For samples named A and B hereafter, LPCVD was used to deposit, under the same experimental conditions, a layer of polycrystalline silicon (poly-Si) with thickness of 2 µm at temperature of 525 °C. No poly-Si layer was deposited for sample C. For the three wafers, a silicon dioxide (SiO_2) layer with thickness of 400 nm was then deposited by plasma-enhanced chemical vapor-deposition (PECVD) at low temperature (350 °C). Finally, a 1-µm-thick aluminium layer was deposited and patterned to form an 8-mm-long 50 Ω characteristic impedance coplanar waveguide (CPW) for performing the RF measurement of the produced samples allowing the extraction of their electrical properties. The CPW line is characterized by a central signal linewidth of 38 µm, ground line widths of 208 µm, and a spacing of 18 µm between the signal line and the ground lines.

On-wafer measurements of the CPW line on the three substrates were performed using an Agilent 2-port performance network analyzer (PNA)-X and a pair of ground-signal-ground (GSG) |Z| probes from Cascade Microtech. An on-wafer short-open-load-thru (SOLT) calibration was applied using an RF impedance standard substrate (ISS) to calibrate the system with the port reference planes defined at the probe tips. Then, a de-embedding scheme proposed by Gillon *et al.* [20] to remove the pad parasitics is applied using the measurements of on-wafer thru, reflect, and line structures implemented alongside the CPW line, in a similar approach to a classical thru-reflect-line (TRL) de-embedding.

From the measured de-embedded scattering (S)-parameters an effective resistivity ($\square_{eff}$) up to 10 GHz at room temperature was extracted using the method described in [21]. This latter parameter accounts for the wafer inhomogeneities (i.e., oxide covering and space charge effects) and corresponds to the resistivity that a uniform (without oxide nor space charge effects) silicon wafer should have in order to sustain identical RF substrate losses. In other words, it is the value of the substrate resistivity that is actually seen by the coplanar devices. Therefore, comparing the wafers in terms of their effective resistivity allows isolating the performance of the substrates by getting rid of series losses and skin effect inside conductors. The same CPW lines were also measured under large-signal condition to evaluate the signal distortion induced by the nonlinear properties of the three different studied substrates. Large-signal measurements of the CPW lines were performed on-wafer using a dedicated setup [6] based on an Agilent 4-port PNA-X vector network analyzer. A power calibration at the CPW line input is performed; then, the subtraction (de-embedding) of the attenuation due to the cables and filters between the CPW line and the power detectors is accounted for by measuring a thru line from the ISS.

With the careful selection of filters and attenuators at the source input and at the harmonics output detector, a harmonic distortion (HD) setup is achieved enabling the detection of harmonic levels of a 900-MHz signal as low as −115 dBm for a maximum input power of 25 dBm. A single tone, with a fundamental frequency of 900 MHz, is injected into one port of the CPW line on each substrate. The power of this input tone, that we shall represent as H1, is swept from −30 to +25 dBm using 50Ω□reference port impedances, and the output signal is

retrieved by a spectrum analyzer. Due to the nonlinear behaviour of silicon-based substrates, signal distortion is introduced and the output signal is in general a multitone signal, with a fundamental component (900 MHz in our case), denoted by H1, along with harmonic components at all integer multiples of this fundamental frequency, denoted by H2, H3, and so on.

To illustrate the degradation of the silicon substrate high resistivity characteristic and its recovery within the introduction of traps at Si/SiO_2 interface, the finite element semiconductor simulation tool ATLAS from Silvaco has been used. ATLAS solves Poisson's and semiconductor equations in the Si-based substrates and at the Si/SiO_2 interfaces, allowing for physical parameters such as fixed oxide charges, interface and volume traps, to be accurately simulated along with their impact on the free carrier distributions in the semiconductor regions. In all simulated substrates an interfacial oxide charge density of 10^{11} cm^{-2} and a nominal Si substrate resistivity of 10000Ω.cm were defined. Tail-type distributions for the acceptor and donor traps were used to model the polysilicon layers according to [22] (characteristic decay energies of 33 meV and edge band state densities of $8x10^{22}$ $cm^{-3}eV^{-1}$).

For TEM characterizations, cross-sectional TEM thin foils were prepared using a dual-beam Scanning Electron Microscope/Focused Ion Beam (SEM/FIB) instrument (FEI Helios Nanolab 650) with the "lift-out" procedure. In order to perform statistical analysis of the grain size distribution and the character of the GBs, Automated Crystal Orientation Mapping in TEM (ACOM-TEM) measurements have been performed with the NanoMegas ASTAR system [23, 24] in a FEI Tecnai G2 F20 TEM operated at 200 kV. For the ASTAR data acquisition, probe and step sizes of 2-nm as well as a precession angle of 0.4^{o} have been used. The ACOM-TEM data have been analyzed using the OIM TSL software from EDAX Inc. A FEI Titan 80-300 "cubed" microscope with aberration correctors for imaging and probe was used to reveal the atomic structure of the GB. In order to allow easy visualization of GB dislocations, local g-maps were obtained using an image processing technique sensitive to small displacements of the lattice fringes in high-angle annular dark-field scanning transmission electron microscopy (HAADF-STEM) images. In order to reduce the influence of instabilities and scanning effects, 15 images are acquired with a low dwell time of 0.4 μs. The images are aligned through a cross-correlation procedure and summed, so that an image with good signal-to-noise ratio and reduced scanning effects is obtained.

3. Results and discussion

3.1 Electrical properties

Figure 1 shows the simulated resistivity profile in the silicon substrate without (Fig. 1a, 1b and 1c) and with (Fig. 1d, 1e, 1f) a poly-Si layer underneath the silicon dioxide. The resistivity profiles are simulated at different static bias conditions for both types of substrate to trigger either inversion, flat band or accumulation regime at the SiO_2-Si interface. High-resistivity wafer (similar to sample C) suffers from the parasitic surface conduction (PSC) effect [21, 25] by which fixed oxide charges present at the SiO_2/Si boundary induce a highly conductive layer at this interface. The resistivity profile is therefore strongly inhomogeneous, as depicted by the curves in Fig. 1b and 1c. Trap-rich substrates (similar to samples A & B) propose a solution to

the PSC effect by introducing a thin poly-Si layer between the oxide layer and the silicon bulk[5]. The numerous traps present in this layer capture the free carriers at the SiO_2/Si interface, suppressing the PSC layer by pinning the surface region in a highly resistive depletion state defined by a deep position of the Fermi-level. Fig. 1e and 1f demonstrate the much weaker dependence of the substrate resistivity with the applied static bias and more importantly very high resistivity values are conserved at the SiO_2/Si interface. These simulations illustrate the high efficiency of the trap-rich layer concept to recover the high resistivity characteristics of the silicon substrate.

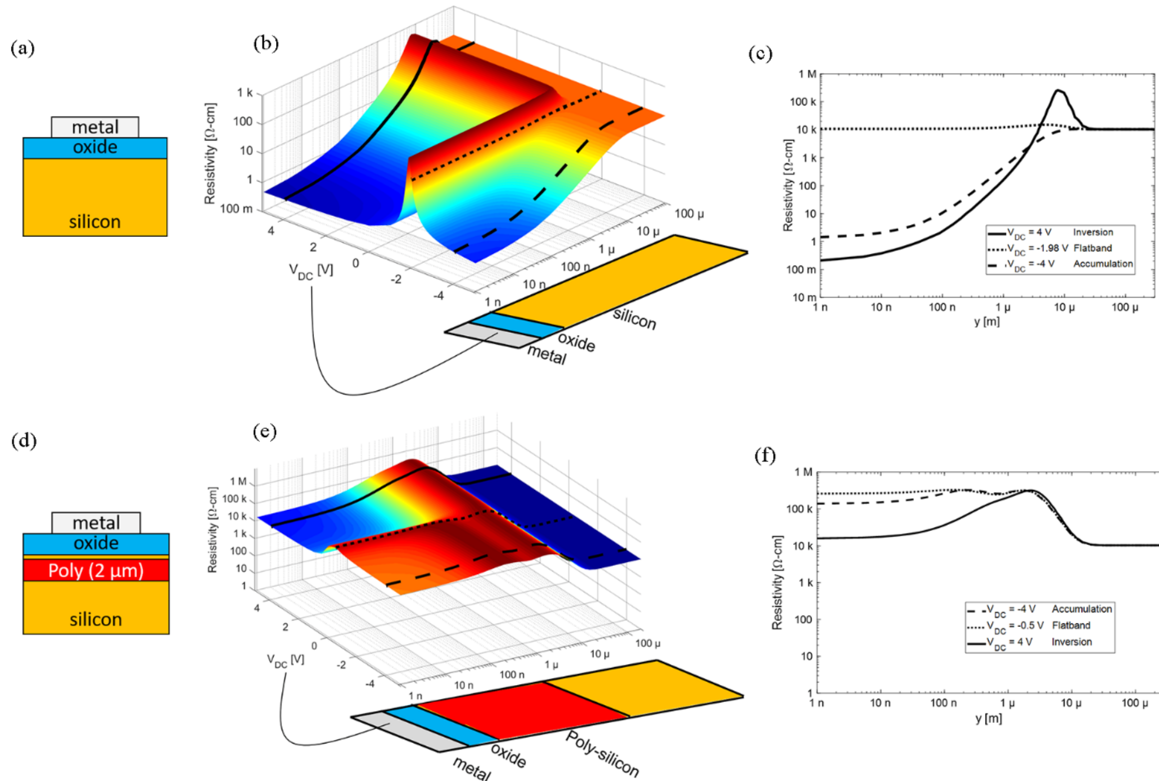

Figure 1. Simulation of the substrate resistivity profile underneath the oxide layer for a high resistivity monocrystalline silicon substrate without (Fig. 1a, 1b, 1c) and with (Fig. 1d, 1e, 1f) a poly-Si layer of 2 µm-thick. In all simulated substrates an interfacial oxide charge density of $1x10^{11}$ cm^{-3} was defined and tail-type distributions for the acceptor and donor traps (characteristic decay energies of 33 meV and edge band state densities of $8x10^{22}$ $cm^{-3}eV^{-1}$) were used to model the polysilicon layers.

Table 1 summarizes the extracted electrical properties based on the high frequency measurements described in the previous section. 10 CPW lines were measured on each substrate and the mean value and standard deviation for the effective resistivity and second harmonics distortion were calculated. As expected, sample C presents a quite low effective resistivity and a high distortion level due to the PSC effects. However, although both substrates including the poly-Si trapping layer, i.e. samples A & B, which were processed following the same fabrication steps one can observe important differences in terms of electrical characteristics. Sample B presents a much higher effective resistivity and lower second

harmonics level than Sample A. Sample B can be considered as an ideal lossless and quite linear silicon-based substrate whereas Sample A might not fulfil the RF specifications for building high quality modern RF ICs. Hereafter, advanced TEM techniques are used to explore the physical reasons of this unexpected different electrical behaviour between samples A and B.

Table 1. Nominal resistivity, effective resistivity extracted from RF small-signal propagating along the CPW line in a frequency range from 100 MHz up to 10 GHz, and the second harmonics distortion level for a fundamental component H1 at 900 MHz and at a power level of +15 dBm.

	Nominal resistivity of handle Si substrate	Effective resistivity	Second harmonics
Sample A	> 10000 Ω.cm	3000 ± 0.1 Ω.cm	-67.5 ± 0.6 dBm
Sample B	> 10000 Ω.cm	24000 ± 0.5 Ω.cm	-94.9 ± 1.3 dBm
Sample C	> 10000 Ω.cm	80 ± 2 Ω.cm	-49.2 ± 0.5 dBm

3.2 TEM characterizations

- Statistical analysis of grain size and type of GBs

Figures 2a and 2b show bright-field TEM (BF-TEM) images of cross-sectional FIB foils prepared on samples A and B, respectively. From these two images and the corresponding selected area electron diffraction (SAED) patterns shown in the inset of the same figures, it can be seen that in both samples, the microstructure exhibits a morphological texture with columnar grains parallel to the growth direction. Some of the grains contain very fine parallel planar defects (white arrows in Fig. 2a and 2b). However, because of the low resolution, the nature of these defects (e.g., nanotwins or stacking faults) cannot be concluded from Fig. 2 but was elucidated using high resolution TEM (HRTEM) as will be shown later. Few dislocations were occasionally observed in the films (black arrows in Fig. 2). Also from Fig. 2 it can be qualitatively observed that the grain size is ranging from 100 nm to 1 μm. At the poly-Si film/Si substrate interface, a very small band (< 100 nm) composed of nanosized grains can be clearly observed in the two poly-Si films (see regions delimited by white dashed lines at the film/substrate interfaces in Fig. 2). Fine details on the microstructure of these bands have been revealed using HRTEM (see next sections). At this stage, clear difference of the microstructure of the poly-Si films A and B cannot be detected in the BF-TEM images of Fig. 2. ACOM-TEM was thus used in order to investigate differences in grain size distribution, GB character and crystallographic orientation in a more quantitative manner.

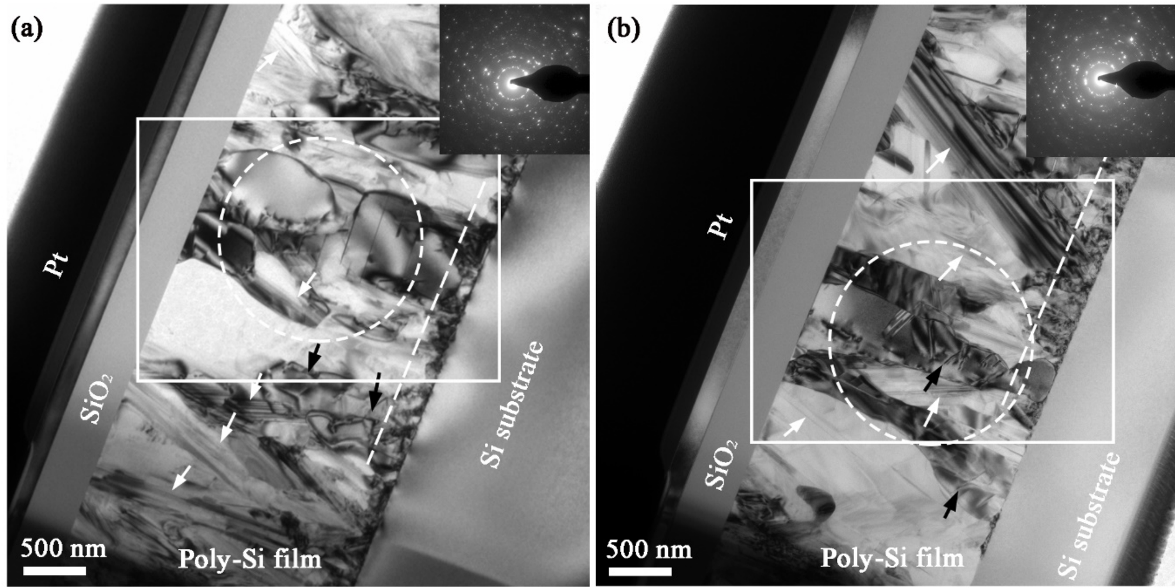

Figure 2. BF-TEM images of FIB cross-sectional foils prepared on Sample A (a) and Sample B (b). The SAED patterns shown in the inset were obtained in regions indicated by white circles. Parallel planar defects and dislocations are marked by white and black arrows, respectively. The white rectangles indicate regions in which the ACOM-TEM maps of Fig. 3 were obtained.

Figures 3a and 3c show typical ACOM-TEM orientation maps obtained in Samples A and B, respectively (regions delimited by white rectangles in Fig. 2a and 2b). Statistical analysis of the grain size distribution and the crystallographic texture performed in several ACOM-TEM maps did not reveal clear differences in the two films (see Figs. S1 and S2 in supplementary materials). Figs. 3b and 3d show the statistical distribution of the length fraction of GBs obtained from the respective regions and the film/substrate interface. For the whole regions, it can be seen that the microstructure of the two films is dominated by random high angle GBs. A high length fraction of $\sum 3$ twins (more than 20%) is also found in both poly-Si films. Previous works also reported the presence of $\sum 3$ twins in poly-Si [7, 26]. The GBs at the interface will be analyzed in next section. It should also be noted that the CSL distributions shown in Fig. 3 are slightly different from those observed by Ratanaphan *et al*. [26] using electron backscatter diffraction (EBSD) in cast poly-Si. Indeed, these authors reported the presence of $\sum 5$ and $\sum 29a$ CSL GBs not observed in the present work while $\sum 7$ and $\sum 27a$ CSL GBs observed in Fig. 3 were not reported by Ratanaphan *et al.* [26]. Such differences can be attributed to the different methods used to produce the poly-Si samples. Based on the results shown in Fig. 3 as well as in Figs. S1 and S2, clear differences of the microstructure between the two films cannot be detected using the ACOM-TEM technique. Other defects present in the films such as SFs or narrowly separated nanotwins (Fig. 2) could play an important role in the electrical behaviour. However, due to their small thickness, these defects can be hardly detected by ACOM-TEM. Furthermore, SFs and nanotwins often introduce streaking of the diffraction spots (see also next section), leading to a drastic decrease of the reliability of the ACOM-TEM maps (the reliability maps of the two films are show in Fig. S3). Similar features can also be expected at the film/substrate interfaces (Fig. 2). In the following section, dedicated

HRTEM experiments are presented in order to investigate the nanoscale planar defects present within the large grains and at the film/substrate interface.

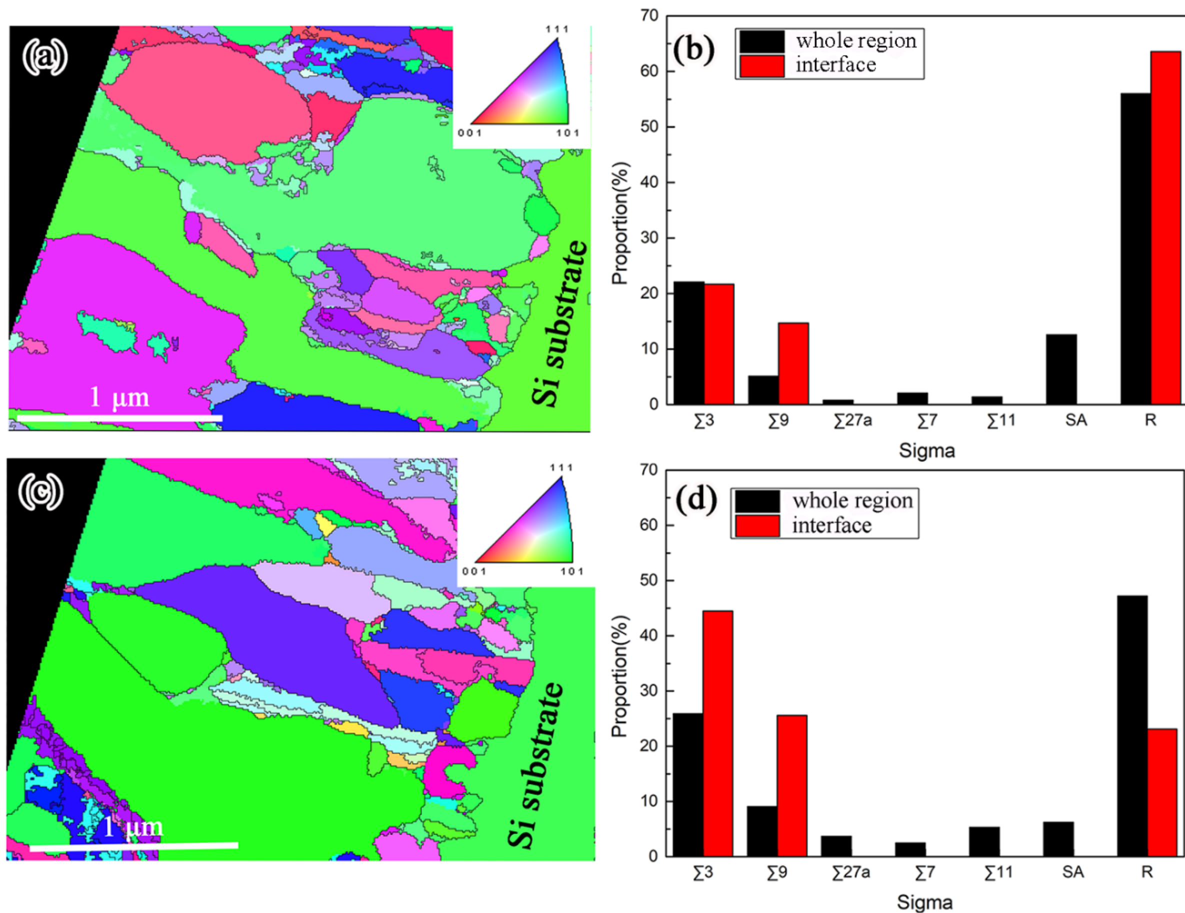

Figure 3. (a and c) ACOM-TEM coloured orientation maps in Samples A and B, respectively, with inverse pole figure (IPF) as inset and (b and d) corresponding proportion of CSL GBs, SA and R-GBs.

- *Nanoscale analysis of defects and interfaces*

Figures 4a and 4d show BF-TEM images obtained in the 'large' grains in the film interior of Samples A and B, respectively. The SAED patterns shown in the inset of these figures were obtained in regions indicated by white circles in the same figures and oriented along the [110] zone axis. Note that these two selected grains contain a high density of very thin lamellae. The diffraction patterns confirm the presence of ∑3 twin boundaries (TBs) as evidenced by the typical superposition of two <110> diffraction patterns mirrored with respect to the {111} plane. The observed streaking of the diffraction spots along the <111> direction is attributed to the presence of edge-on stacking faults (SFs) and/or a high density of very thin lamellar twins. Figs. 4b and 4e show typical filtered high-resolution TEM images and corresponding fast Fourier transform (FFT) patterns of nano-twins in Samples A and B, respectively. It can be seen in these figures that the nanostructure consists on nano-sized twins with sharp and atomically flat ∑3 {111} coherent twin boundaries (CTBs). The twin thickness in both films is ranging from 1.5 nm to 12 nm. Few SFs have been occasionally observed (labelled S in Figs. 4c and 4f). Similar features have been observed in other grains. Statistical HRTEM

measurements in several grains did not reveal a clear difference of the twin thickness in both films. We thus believe that nanotwins formed within the 'large' grains in the film interior cannot be considered as responsible for the different electrical behaviour of the two poly-Si films. In the following paragraphs, the focus will be on the nanostructure of the small bands observed at the film/substrate interface shown in Figs. 2a and 2b.

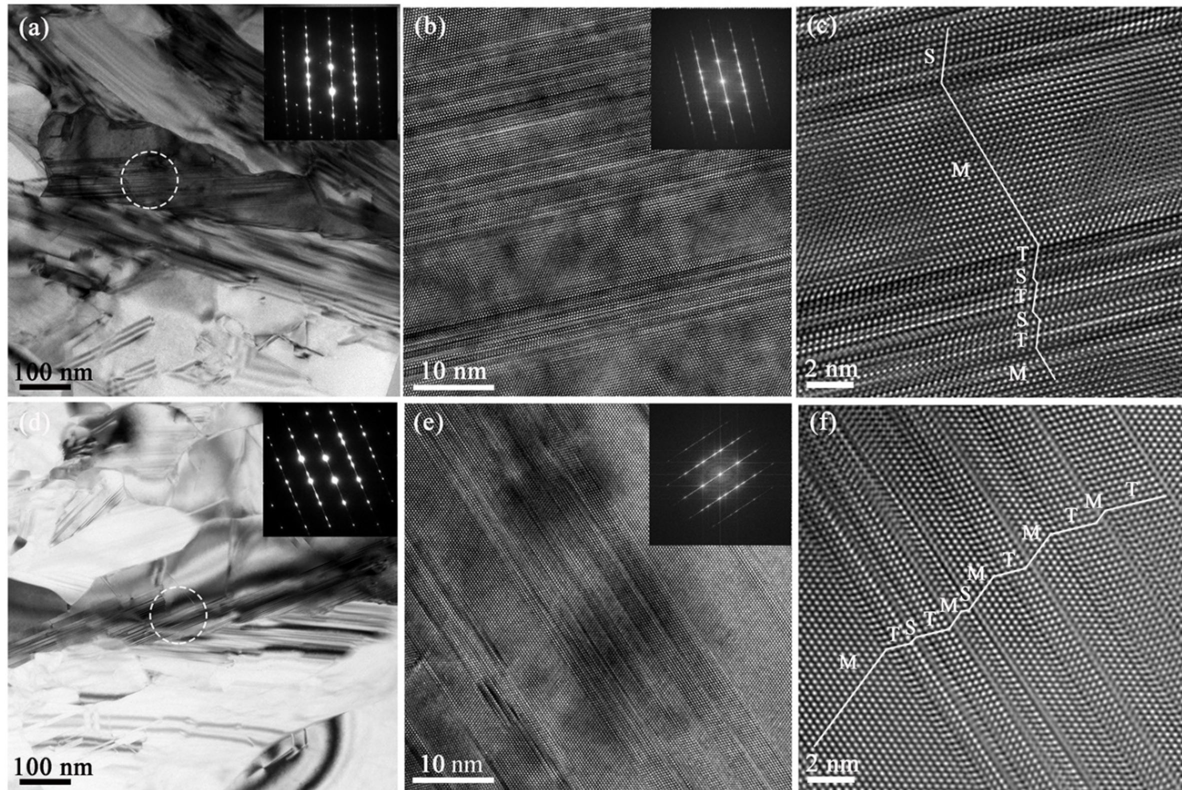

Figure 4. (a and d) Bright field TEM images of planar defects formed within large grains in the poly-Si layers of Sample A and B, respectively. The SAEDs shown in the insets were obtained in regions indicated by white circles in the same figures. HRTEM images (b and e) and enlarged filtered images (c and f) showing nano-twins and SFs in the two samples. Changing of stacking sequences are marked by white lines. The letters M, T and S correspond to the matrix, twin and stacking fault, respectively.

The BF-TEM images of Figs. 5a and 5c reveal the microstructure at the film/substrate interfaces in Sample A and Sample B, respectively. Figs. 5b and 5d are the enlarged BF-TEM images of the interfaces marked by the white boxes in Figs. 5a and 5c. These images show that the interface in both films consists of nanosized grains (120-150 nm). However, in contrast with Sample A in which only few nanotwins connect to the film/substrate interface (black arrows in Fig. 5a), grains at the film/substrate interface in Sample B exhibit a large amount of nanotwins including numerous multi-fold nanotwins (black arrows in Fig. 5c). Furthermore, it can be observed in Fig. 5 that the film/substrate interface in Sample A is quite smooth (Figs. 5a and 5b) while the same interface in Sample B exhibits very large number of nanoscale facets (Figs. 5c and 5d), not observed in Sample A. Similar behaviour was observed in all the analyzed

TEM images (see Fig. S4 in supplementary materials for other examples). At this stage, it can be expected that the higher effective resistivity and lower harmonics distortion (Table 1) of Sample B is due to the film/substrate interface in which huge amounts of planar defects are confined. In the following, both conventional HRTEM and Cs aberration corrected HAADF-STEM techniques are used to confirm this assumption and to investigate the nature of the defects at the nanoscale.

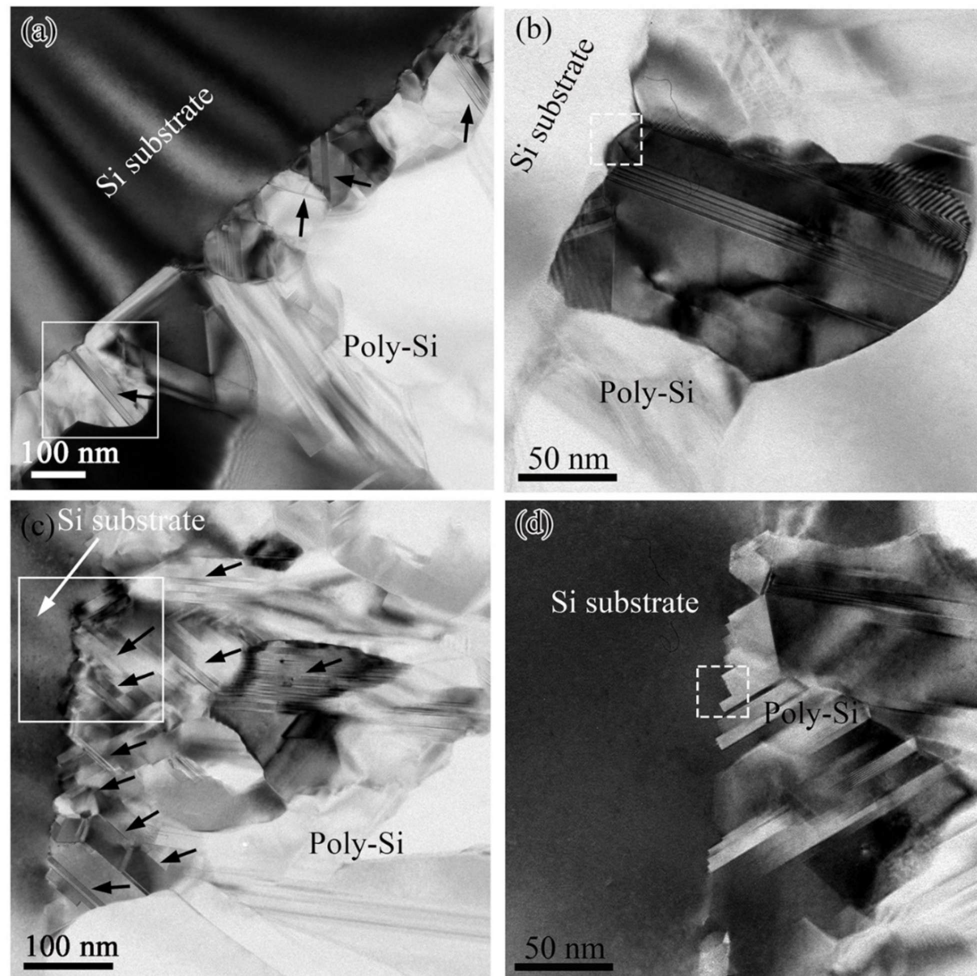

Figure 5. Bright-field TEM images of nanocrystalline grains formed at the poly-Si/Si substrate interface of Sample A (a,b) and B (c,d). (b) and (d) are the enlarged BF-TEM images of the interfaces marked by the white boxes in a and c. Few nanotwins connected to the film/substrate interface are marked by black arrows in (a) while a large amount of these nanotwins is present in (c). Note also the faceted aspect of the interface in (c) and (d) in contrast with the more smooth character of the interface in (a) and (b). The dashed squares in (b) and (d) are the regions selected for HRTEM observation shown in Figure 6.

HRTEM images obtained at the poly-Si film/Si substrate interface in Sample A show that, in most cases, this interface exhibits a smooth morphology and a random character (Figs. 6a and 6b). However, in Sample B, the interface exhibits a large amount of nanoscale facets (Fig. 6c) that can be identified as $\sum3\{111\}$ CTBs and $\sum3\{112\}$ incoherent TB (ITBs) with a $\sum3$

misorientation relationship between the film and the substrate (Fig. 6d). The height of these facets is ranging from 3 to 42 nm. Both observations are characteristic for the respective sample. This is in agreement with statistical analysis of the character of the film/substrate interface by ACOM-TEM results showed in Fig.3b and 3d. Indeed, these measurements have shown that, in Sample A, the fraction of random high angle GBs, ∑3 and ∑9 GBs at the film/substrate interface are 63.6%, 21.7% and 14.7%, respectively, while these values change to 23.1%, 44.5% and 25.6% at the same interface of Sample B (see Figures 3b and 3d). Low angle GBs were not observed at the interfaces. Cs aberration corrected HAADF-STEM image and corresponding FFT pattern of ∑3{111}-∑3{112} facets of Sample B are shown in Fig. 7a. The enlarged HAADF-STEM image of ∑3{112} ITB in Fig. 7b shows that the periodic structural unit of this twin boundary consists of 7, 5 and 6 membered rings in agreement with previous HRTEM observations [27]. The incoherent character of the ∑3{112} ITB can be clearly seen in the local **g** map of Fig. 7c with an array of interfacial dislocations located at the twin/matrix interface. In contrast with ∑3{111} CTBs which are electrically inactive [17], the presence of interfacial dislocations at ∑3{112} ITBs is expected to be at the origin of the electrical activity of these boundaries [10, 28]. In addition of ∑3{111} and ∑3{112} TBs, a high density of nanoscale faceted ∑9 GBs was observed in Sample B. Fig. 7d exhibits a HAADF-STEM image and corresponding FFT pattern of ∑9(122) and ∑9(114) GBs. It can be seen in Fig. 7e that the structural unit of the ∑9{122} GB consists of 7 and 5 membered rings [29]. The atomic structure of the ∑9{114} GB was recently reported in the literature [30, 31], but its structural units are still under investigation. The local **g** map of the ∑9{114} GB contains an array of GB dislocations as indicated in Fig. 7f. However, only few dislocations are observed at the ∑9{122} GB. This is in agreement with previous work showing that this GB has a relatively low energy configuration often accompanied with very few dislocations and local distortions [29].

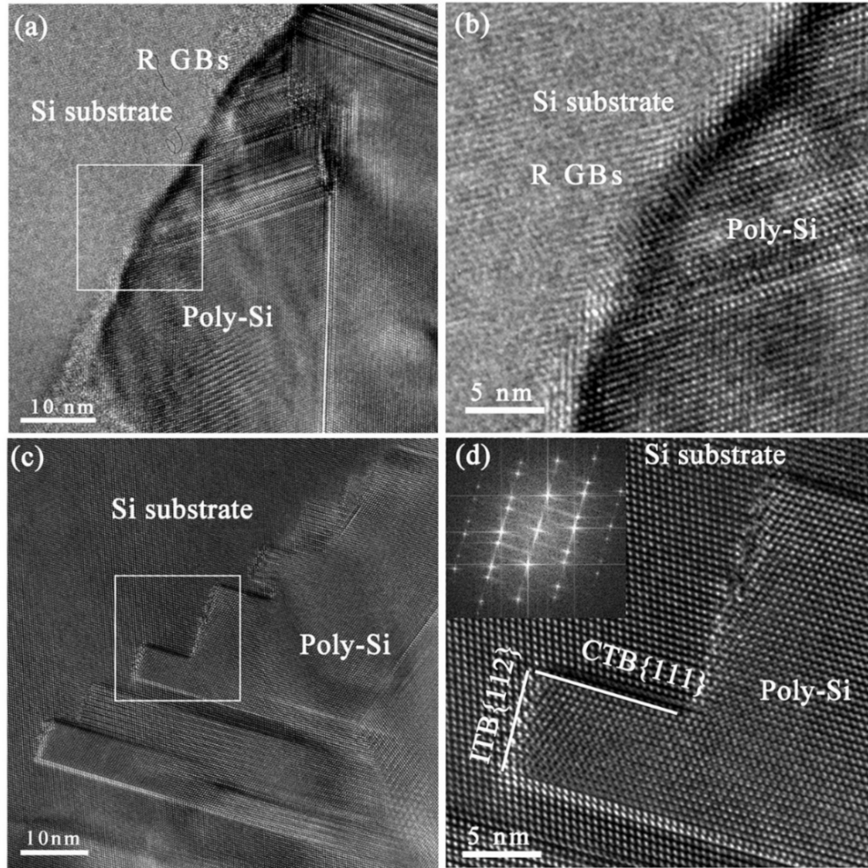

Figure 6. Conventional HRTEM images showing random GBs at the the poly-Si/Si substrate interface of Sample A (a) and ∑3{111}-∑3{112} facets in Sample B (c). (b) and (d) are the enlarged HRTEM images from the white squares in (a) and (c), respectively. An FFT pattern of (d) is inserted in the upper-left corner.

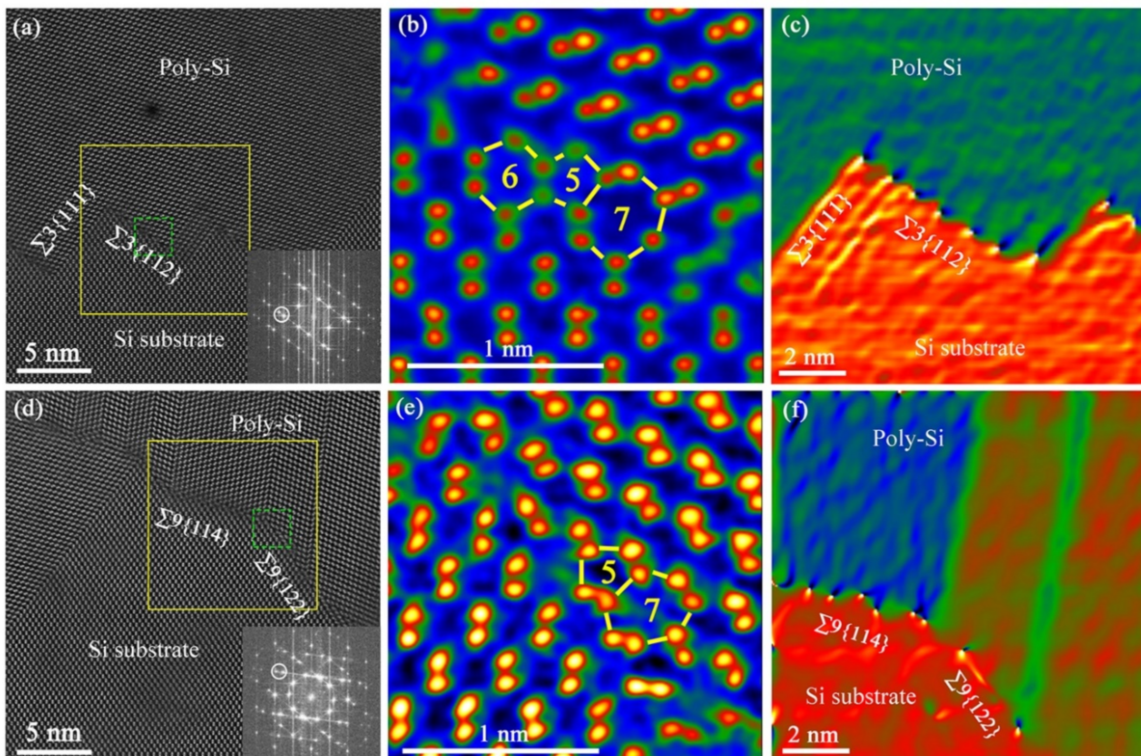

Figure 7. Aberration corrected HAADF-STEM images (<110> zone axis) of the ∑3{111}-∑3{112} facets (a) and ∑9 GBs (d) formed at the poly-Si film/Si substrate interface in Sample B. (b) and (e) are enlarged HAADF-STEM images of ∑3{112} TB and ∑9 {122} GB marked by the green dotted box in (a) and (d). (c) and (f) are local-**g** maps of the GBs presented in the yellow boxes in (a) and (d). The maps are obtained using the spots indicated by a white circle on the FFT in the right corner of (a) and (d).

In the literature it is argued that the interaction of twins could lead to the formation of various multiple twins and GBs with similar character but with different GB planes [30]. Fig. 8a shows a complex ∑3 multiple twin pattern formed at the film/substrate interface of Sample B. More details of such a feature can be seen in the high resolution HAADF-STEM image of Fig. 8b. In this figure, a fivefold twin can be observed. The formation of such a defect can be attributed to the nucleation, migration and interaction of ∑3{111} CTBs [32]. Generally, the ideal angle between two {111} planes in an fcc structure is 70.53°, leaving an angular gap of ~7.4° when forming a fivefold twin. As shown in Fig. 8b, the angles between ∑3{111} CTBs are larger than 70.53°, and the deviation between the maximum and the minimum angle is only 2.9°, indicating that the 7.4° gap is shared by the different twins forming the fivefold twin. Similar behaviour has been reported in nanocrystalline materials [33, 34]. In Fig. 8b, an extrinsic stacking fault can be observed as indicated by changes of the stacking sequence marked by the white arrow in the same figure. This SF is also visible in Fig. 8c. In Fig. 8b, it can also be observed that, in addition to the ∑3{111} and ∑3{112} facets, the film/substrate interface also involves ∑3(124)(344) GBs. Furthermore, a ∑3(122)(112) GB forming a triangle with two ∑3{111} CTBs of the fivefold twin can be observed in the white square in Fig. 8b. It is worth noting here that this type of ∑3 GB has not been reported before in the literature. An enlarged HAADF-STEM image of this GB is shown in Fig. 8c and in which strong distortions can be observed within the atomic structure of this GB as evidenced by the dumbbells marked by red ellipses. Indeed, these dumbbells exhibit a completely different orientation, which cannot be assigned to one of the two grains. Furthermore, some single-atomic columns are clearly observed as indicated by green circles in Fig. 8c. These observations are in agreement with the high number of dislocations decorating this GB in the local **g** map of Fig. 8d. Such feature could significantly affect the electrical activity of this class of GBs. Twins interaction could also lead to the formation of $\Sigma 3^n$ GB, such as ∑9 GBs. Fig. 9a shows a typical case of a ∑9 GB generated from the interaction of two ∑3 twins. Indeed, it can be seen in this figure that a ∑9(114) GB has been formed at the junction between two ∑3 nanotwins following the "∑3 regeneration model" ∑3 + ∑3= ∑9 [35]. Moreover, dissociation of a ∑9 GB into ∑3 GBs was observed in the HAADF-STEM image of Fig. 9b showing a ∑9(114) GB connected to a nanosized triangular grain delimited by ∑3(111), $\Sigma 3(11\bar{1})$ and ∑3(211) TBs. It has been already shown in the literature that, in order to reduce the total boundary energy, ∑9 GB dissociates following the reaction: ∑9{114} = ∑3{111} + ∑3{111} [16, 36].

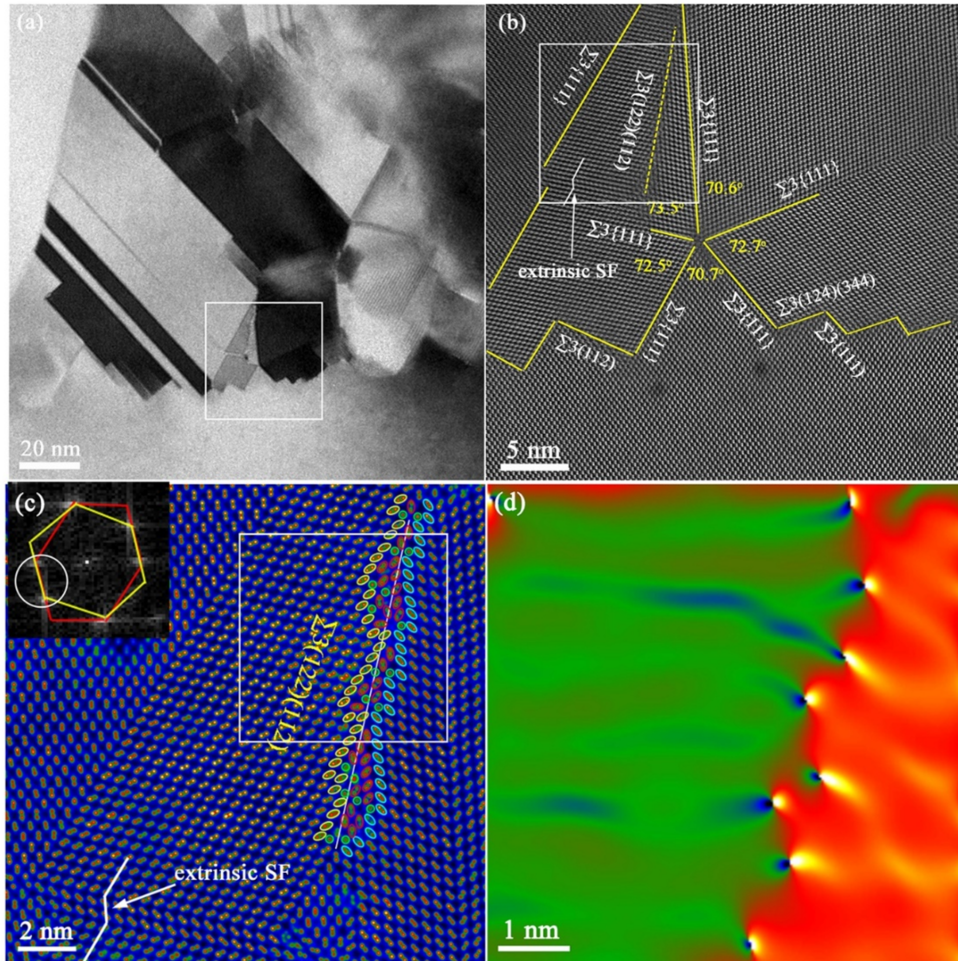

Figure 8. (a) BF-TEM image of the multiple twins formed at the interface of Sample B; (b) HAADF-STEM image (<110> zone axis) from the region indicated by white square in (a); (c) enlarged HAADF-STEM image of ∑3(122)(112) GB in the white square of (b). Dumbbell columns from to the left grain are marked by yellow ellipses while columns from the right grain are marked by blue ellipses. The dumbbells marked by red ellipses deviate from the ideal orientation and cannot be assigned to one of the two grains. Single Si atomic columns are marked by green circles. Change of the stacking sequence is marked by white line. (d) Local g map of ∑3(122)(112) GB presented in the white square of (c). The map is obtained using the spots indicated by a white circle in the inset.

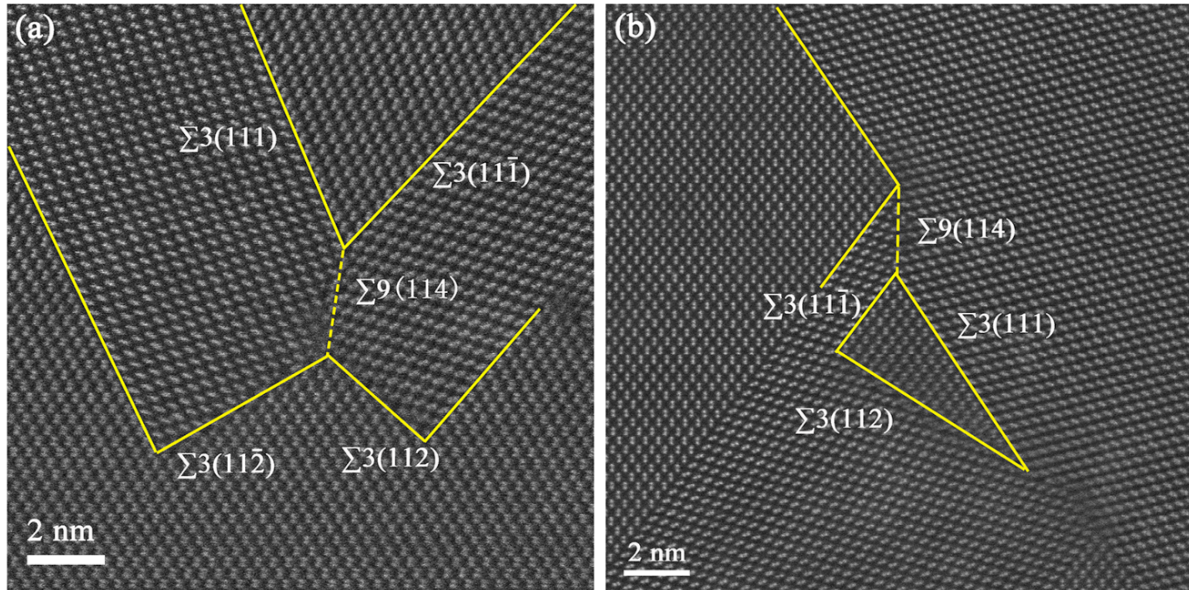

Figure 9. HAADF-STEM images (<110> zone axis) showing the generation (a) and dissociation (b) of the ∑9 GBs at the interface of Sample B. The ∑9 GBs are marked by yellow dashed lines while ∑3 GBs are marked by yellow lines.

Based on the present extensive TEM characterizations, it can be concluded that the high resistivity characteristic and high electrical linearity of Sample B is controlled by the huge amount of defects confined at the poly-Si/Si substrate interface. Indeed, it was demonstrated that this interface exhibits a ∑3 twin-like character with nanoscale facets alternating between ∑3{111} CTBs and ∑3{112} ITBs. The interaction between nanotwins with different orientations leads to the formation of complex patterns of multifold twins and numerous ∑3 CSL and ∑9 GBs including ∑3(124)(344) GB, ∑3(122)(112) GB, ∑9(122) and ∑9(114) GBs. Furthermore, the forward and backward transformations between ∑3 TB and ∑9 GB increase of the complexity of the GBs pattern. Interestingly, many CSL GBs have been observed to deviate from their ideal crystallographic plane leading to the formation of extrinsic GB defects (Fig. 8). Such behaviour can be attributed to the high internal stress arising from the confinement of such a large amount of extended defects in a small volume. It is worth noting that the carrier trapping capacity in trap layer is not only linked to the type of grain boundaries, but also the density of defects at interface [18, 19]. A high density of the interfacial defects leads to significant increase of the electrical resistivity of the poly-Si films. In contrast, sample A exhibits a poly-Si/Si substrate interface with more random character and few nanoscale twins which could explain the low electrical resistivity observed in this sample. It is also worth noting that significant differences between the two samples in terms of grain size distribution, crystallographic texture as well as nanotwins or stacking faults formed in the interior of the Poly-Si films were not observed. However, the origin of the difference between the nature of the poly-Si/Si substrate interface in the two films remains obscure at this stage. These differences probably result from slight difference in surface quality of substrate or slight difference in LPCVD parameter, etc. Further investigations are needed to elucidate such feature.

4. Conclusions

In summary, thanks to advanced TEM characterizations we demonstrate that the high resistivity characteristic and high electrical linearity of poly-Si films are strongly controlled by the ∑3 twin type character of the poly-Si/Si substrate interface. Indeed, this feature leads to the generation of a huge amount of stacking faults, ∑3 CTBs and ITBs, ∑9 GB and multi-fold twins. The interaction between different types of interfaces increases the complexity of the microstructure with the formation of common and less common GBs confining a high density of interfacial dislocations. These defects can effectively capture a large amount of induced carriers at that interface which is located underneath ICs built on any type of silicon-based substrates. This finding gives guidelines to technologists for developing high quality Si-based substrates for RF applications by favouring the formation of ∑3 twin-type interface between poly-Si layers and Si substrate. On-going experiments are underway in order to elucidate the physical parameters and the mechanism(s) controlling the formation of the ∑3 twin-type Poly-Si/Si substrate interface.

Acknowledgements

H. Idrissi is mandated by the Belgian National Fund for Scientific Research (FSR-FNRS).

Data availability

The raw/processed data required to reproduce these findings cannot be shared at this time as the data also forms part of an ongoing study.

References

[1] A. Green Martin, Silicon solar cells: state of the art, Philos. T. R. Soc. A. 371(1996) (2013) 20110413.
[2] L. Seok-Woon, J. Seung-Ki, Low temperature poly-Si thin-film transistor fabrication by metal-induced lateral crystallization, IEEE Electr. Device L. 17(4) (1996) 160-162.
[3] S.D. Brotherton, Polycrystalline silicon thin film transistors, Semicond. Sci. Tech. 10 (1995) 721-738.
[4] V. Mosser, J. Suski, J. Goss, E. Obermeier, Piezoresistive pressure sensors based on polycrystalline silicon, Sensor. Actua. A: Phys. 28(2) (1991) 113-132.
[5] D. Lederer, J. Raskin, New substrate passivation method dedicated to HR SOI wafer fabrication with increased substrate resistivity, IEEE Electr. Device L. 26(11) (2005) 805-807.
[6] C.R. Neve, J. Raskin, RF Harmonic Distortion of CPW Lines on HR-Si and Trap-Rich HR-Si Substrates, IEEE Trans. Electr. Devices 59(4) (2012) 924-932.
[7] L. Haji, P. Joubert, J. Stoemenos, N.A. Economou, Mode of growth and microstructure of polycrystalline silicon obtained by solid-phase crystallization of an amorphous silicon film, J Appl. Phys. 75(8) (1994) 3944-3952.
[8] J. Viatella, R.K. Singh, Transient recrystallization of amorphous silicon films, Mater. Sci. Eng. B 47(1) (1997) 78-86.
[9] X.-Z. Bo, N. Yao, S.R. Shieh, T.S. Duffy, J.C. Sturm, Large-grain polycrystalline silicon films with low intragranular defect density by low-temperature solid-phase crystallization without underlying oxide, J Appl. Phys.91(5) (2002) 2910-2915.

[10] J. Chen, T. Sekiguchi, D. Yang, F. Yin, K. Kido, S. Tsurekawa, Electron-beam-induced current study of grain boundaries in multicrystalline silicon, J Appl. Phys. 96(10) (2004) 5490-5495.
[11] B. Chen, J. Chen, T. Sekiguchi, M. Saito, K. Kimoto, Structural characterization and iron detection at Σ3 grain boundaries in multicrystalline silicon, J Appl. Phys. 105(11) (2009) 113502.
[12] A. Stoffers, B. Ziebarth, J. Barthel, O. Cojocaru-Miredin, C. Elsasser, D. Raabe, Complex Nanotwin Substructure of an Asymmetric Sigma9 Tilt Grain Boundary in a Silicon Polycrystal, Phys. Rev. Lett. 115(23) (2015) 235502.
[13] J. Chen, T. Sekiguchi, D. Yang, Electron-beam-induced current study of grain boundaries in multicrystalline Si, phys. status solidi (c) 4(8) (2007) 2908-2917.
[14] J. Chen, T. Sekiguchi, R. Xie, P. Ahmet, T. Chikyo, D. Yang, S. Ito, F. Yin, Electron-beam-induced current study of small-angle grain boundaries in multicrystalline silicon, Scr. Mater. 52(12) (2005) 1211-1215.
[15] A. Bary, G. Nouet, Electrical activity of the first- and second-order twins and grain boundaries in silicon, J Appl. Phys. 63(2) (1988) 435-438.
[16] H.Y. Wang, N. Usami, K. Fujiwara, K. Kutsukake, K. Nakajima, Microstructures of Si multicrystals and their impact on minority carrier diffusion length, Acta Mater. 57(11) (2009) 3268-3276.
[17] V.A. Oliveira, B. Marie, C. Cayron, M. Marinova, M.G. Tsoutsouva, H.C. Sio, T.A. Lafford, J. Baruchel, G. Audoit, A. Grenier, T.N. Tran Thi, D. Camel, Formation mechanism and properties of twinned structures in (111) seeded directionally solidified solar grade silicon, Acta Mater. 121 (2016) 24-36.
[18] C. Donolato, The relation between EBIC contrast and recombination velocity of a grain boundary, Mate.r Sci. Engin. B 24 (1994) 61-63.
[19] W. Seifert, G. Morgenstern, M. Kittler, Influence of dislocation density on recombination at grain boundaries in multicrystalline silicon, Semicond. Sci. Technol. 8 (1993) 1687-1691.
[20] R. Gillon, J. Raskin, D. Vanhoenacker, J. Colinge, Determining the reference impedance of on-wafer TLR calibrations on tossy substrates, 1996 26th European Microwave Conference, 1996, 170-173.
[21] D. Lederer, J.-P. Raskin, Effective resistivity of fully-processed SOI substrates, Solid-State Electron. 49(3) (2005) 491-496.
[22] M. Kemp, M. Meunier, C.G. Tannous, Simulation of the amorphous silicon static induction transistor, Solid-State Electron. 32(2) (1989) 149-157.
[23] B. Amin-Ahmadi, D. Connetable, M. Fivel, D. Tanguy, R. Delmelle, S. Turner, L. Malet, S. Godet, T. Pardoen, J. Proost, D. Schryvers, H. Idrissi, Dislocation/hydrogen interaction mechanisms in hydrided nanocrystalline palladium films, Acta Mater.111 (2016) 253-261.
[24] B. Wang, H. Idrissi, M. Galceran, M.S. Colla, S. Turner, S. Hui, J.P. Raskin, T. Pardoen, S. Godet, D. Schryvers, Advanced TEM investigation of the plasticity mechanisms in nanocrystalline freestanding palladium films with nanoscale twins, Int. J Plasticity (2012) 140-156.
[25] D. Lederer, J.-P. Raskin, Substrate loss mechanisms for microstrip and CPW transmission lines on lossy silicon wafers, Solid-State Electron. 47(11) (2003) 1927-1936.
[26] S. Ratanaphan, Y. Yoon, G.S. Rohrer, The five parameter grain boundary character distribution of polycrystalline silicon, J Mater. Sci. 49(14) (2014) 4938-4945.
[27] N. Sakaguchi, H. Ichinose, S. Watanabe, Atomic Structure of Faceted 3 CSL Grain Boundary in Silicon: HRTEM and Ab-initio Calculation, Mater. Trans. 48 (2007) 2585 - 2589.
[28] J. Huang, S. Varlamov, J. Dore, J.S. Yun, M.A. Green, Micro-structural defects in polycrystalline silicon thin-film solar cells on glass by solid-phase crystallisation and laser-induced liquid-phase crystallisation, Sol. Ener.g Mat. Sol. C 132 (2015) 282-288.

[29] M. Couillard, G. Radtke, G.A. Botton, Strain fields around dislocation arrays in a Σ9 silicon bicrystal measured by scanning transmission electron microscopy, Philos. Mag. 93(10-12) (2013) 1250-1267.
[30] J.L. Batstone, Twin intersections in silicon on sapphire, Philos. Mag. B 63(5) (1991) 1037-1050.
[31] Y. Ohno, K. Inoue, K. Fujiwara, K. Kutsukake, M. Deura, I. Yonenaga, N. Ebisawa, Y. Shimizu, K. Inoue, Y. Nagai, H. Yoshida, S. Takeda, S. Tanaka, M. Kohyama, Impact of local atomic stress on oxygen segregation at tilt boundaries in silicon, Appl. Phys. Lett. 110(6) (2017) 062105.
[32] Y.T. Zhu, J. Narayan, J.P. Hirth, S. Mahajan, X.L. Wu, X.Z. Liao, Formation of single and multiple deformation twins in nanocrystalline fcc metals, Acta Mater. 57(13) (2009) 3763-3770.
[33] P. Huang, G.Q. Dai, F. Wang, K.W. Xu, Y.H. Li, Fivefold annealing twin in nanocrystalline Cu, Appl. Phys. Lett. 95(20) (2009) 203101.
[34] Y.T. Zhu, X.Z. Liao, R.Z. Valiev, Formation mechanism of fivefold deformation twins in nanocrystalline face-centered-cubic metals, Appl. Phys. Lett. 86(10) (2005) 103112.
[35] V. Randle, Twinning-related grain boundary engineering, Acta Mater. 52(14) (2004) 4067-4081.
[36] A. Garg, W.A.T. Clark, J.P. Hirth, Dissociated and faceted large-angle coincident-site-lattice boundaries in silicon, Philos. Mag. A 59(3) (1989) 479-499.

Conflict of interest statement

We declare that we have no financial and personal relationships with other people or organizations that can inappropriately influence our work, there is no professional or other personal interest of any nature or kind in any product, service and/or company that could be construed as influencing the position presented in, or the review of, the manuscript entitled.

Supplementary materials

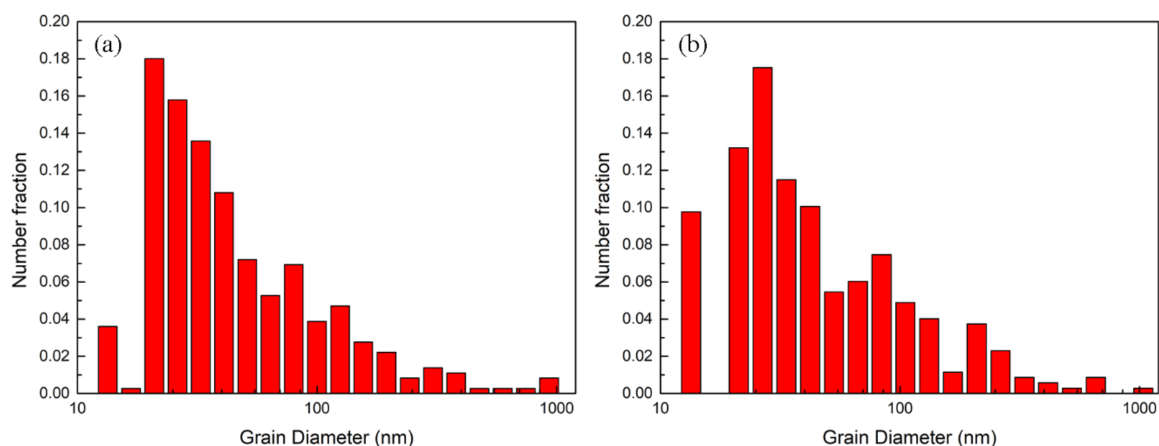

Fig. S1. Grain size distribution from ACOM-TEM measurements in (a) Sample A and (b) Sample B.

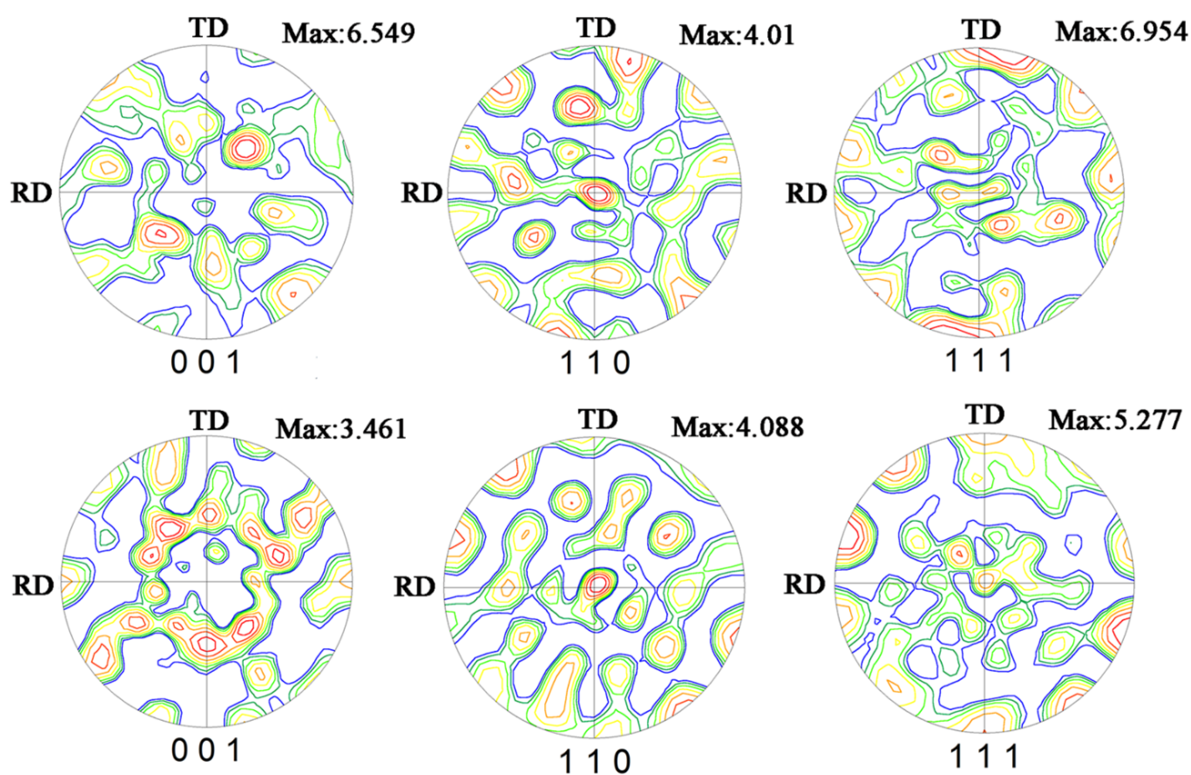

Fig. S2. (001), (110) and (111) pole figures in Sample A and Sample B obtained from the ACOM-TEM maps of Figure 2a and 2c.

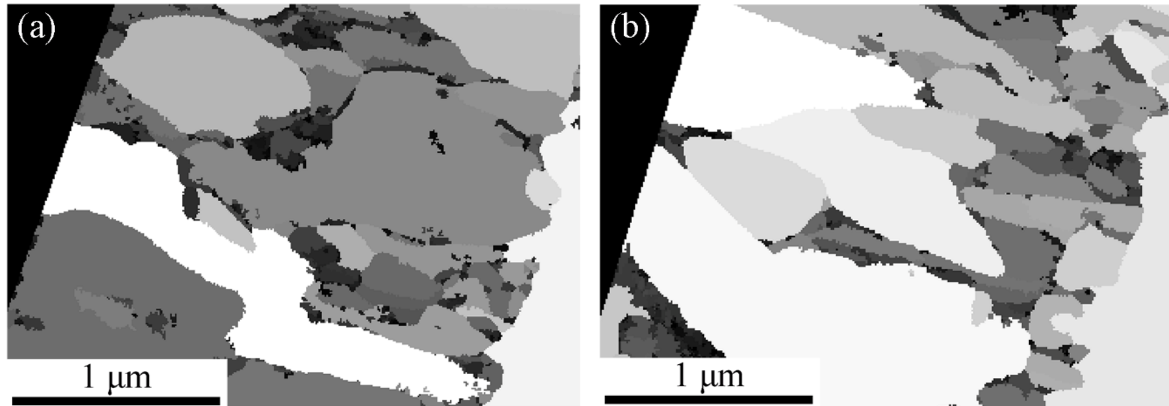

Fig. S3. Reliability map for (a) Sample A and (b) Sample B. The intensity scales proportional to the indexation quality (i.e. from 0% (black) to the maximum of 50% (white)). Note that the low reliability obtained here is probably due to the complex crystallography of the system as well as the highly defective microstructure with a high density of planar defects leading to the presence of streaking of the diffraction spots.

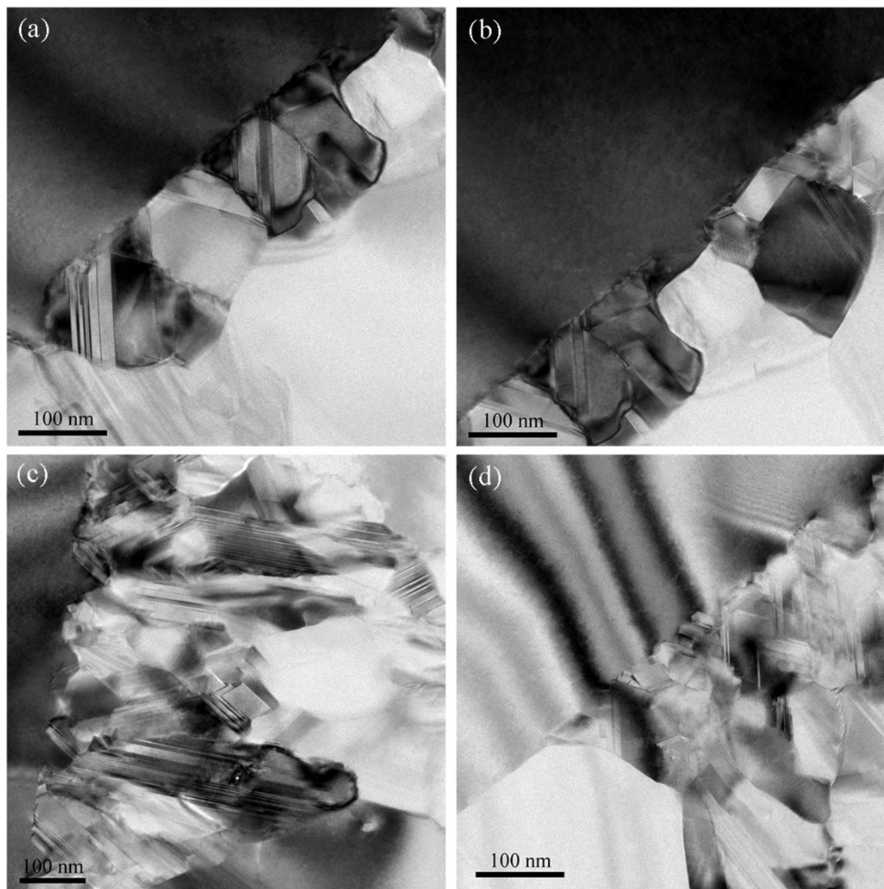

Fig. S4. Extra BF-TEM images of the poly-Si/Si substrate interface obtained in other regions in Sample A (a,b) and B (c,d). These images confirm the difference of the interface between the samples.